Universidade Federal de Campina Grande
Centro de Engenharia Elétrica e Informática
Programa de Pós-Graduação em Engenharia Elétrica

AC-DC-AC Power Conversion Systems for Applications as Unified Power Quality Conditioners.

Jean Torelli Cardoso

Campina Grande - PB, Brasil
August 2024

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Jean Torelli Cardoso

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AC-DC-AC Power Conversion Systems for Applications as Unified Power Quality Conditioners

JEAN TORELLI CARDOSO

TESE APROVADA EM 29/08/2024

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REGISTRO DE PRESENÇA E ASSINATURAS

1. ATA DA DEFESA PARA CONCESSÃO DO GRAU DE DOUTOR EM CIÊNCIAS, NO DOMÍNIO DA ENGENHARIA ELÉTRICA, REALIZADA EM 29 DE AGOSTO DE 2024

(Nº 381)

CANDIDATO(A): **JEAN TORELLI CARDOSO.** COMISSÃO EXAMINADORA: ANTONIO MARCUS NOGUEIRA LIMA, Dr., UFCG - Presidente da Comissão e Examinador Interno, CURSINO BRANDÃO JACOBINA, Dr. Ing., UFCG, Orientador, ALEXANDRE CUNHA OLIVEIRA, D.Sc., UFCG - Examinador Interno, LEONARDO RODRIGUES LIMONGI, Dr., UFPE - Examinador Externo, LUIZ HENRIQUE SILVA COLADO BARRETO, Dr., UFC - Examinador Externo TÍTULO DA TESE: AC-DC-AC Power Conversion Systems for Applications as Unified Power Quality Conditioners. ÁREA DE CONCENTRAÇÃO: Processamento da Energia. HORA DE INÍCIO: **09h00** – LOCAL: **Sala Virtual, conforme Art. 5º da PORTARIA SEI Nº 01/PRPG/UFCG/GPR, DE 09 DE MAIO DE 2022.** Em sessão pública, após exposição de cerca de 45 minutos, o(a) candidato(a) foi arguido(a) oralmente pelos membros da Comissão Examinadora, tendo demonstrado suficiência de conhecimento e capacidade de sistematização, no tema de sua tese, obtendo conceito APROVADO. Face à aprovação, declara o presidente da Comissão, achar-se o examinado, legalmente habilitado a receber o Grau de Doutor em Ciências, no domínio da Engenharia Elétrica, cabendo a Universidade Federal de Campina Grande, como de direito, providenciar a expedição do Diploma, a que o(a) mesmo(a) faz jus. Na forma regulamentar, foi lavrada a presente ata, que é assinada por mim, Leandro Ferreira de Lima, e os membros da Comissão Examinadora. Campina Grande, 29 de Agosto de 2024.

LEANDRO FERREIRA DE LIMA
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JEAN TORELLI CARDOSO

Candidato

2 - APROVAÇÃO

2.1. Segue a presente Ata de Defesa de Tese de Doutorado da candidato **JEAN TORELLI CARDOSO**, assinada eletronicamente pela Comissão Examinadora acima identificada.

2.2. No caso de examinadores externos que não possuam credenciamento de usuário externo ativo no SEI, para igual assinatura eletrônica, os examinadores internos signatários **certificam** que os examinadores externos acima identificados participaram da defesa da tese e tomaram conhecimento do teor deste documento.

Documento assinado eletronicamente por **LEANDRO FERREIRA DE LIMA**, **SECRETÁRIO (A)**, em 30/08/2024, às 09:42, conforme horário oficial de Brasília, com fundamento no art. 8º, caput, da Portaria SEI nº 002, de 25 de outubro de 2018.

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Resumo

Neste trabalho, são analisadas seis configurações ca-cc-ca monofásicas e duas trifásicas que podem operar com melhores níveis de distorção harmônica e eficiência que topologias convencionais dentro de alguns cenários de aplicações. Nesse sentido, esse trabalho teve como objetivos: *i)* propor e analisar configurações ca-cc-ca monofásicas com características multiníveis, ou seja, que possam sintetizar formas de onda multiníveis e menores tensões de bloqueio nos dispositivos semicondutores; *ii)* propor e analisar configurações ca-cc-ca monofásicas, assim como, estratégias de controle que permitam melhorar a performance da estrtura em termos de tensão mínima no barramento CC e compensação série; *iii)* propor e analisar configurações ca-cc-ca trifásicas multiníveis a quatro fios que permitam alcançar melhores desempenhos em termos de tensão mínima no barramento ao operar com cargas severamente desbalaceadas. Os conversores ca-cc-ca monofásicos e trifásicos analisados fornecem uma tensão de saída com amplitude e frequência constantes, além de uma corrente de entrada senoidal com baixo teor harmônico e elevado fator de potência. Além disso, estes conversores estudados podem ser empregados para compensar harmônicos, sobretensões e afundamentos na tensão da rede elétrica, bem como para corrigir a potência reativa e reduzir os harmônicos gerados por cargas não lineares. A metodologia de estudo dessas configurações envolve uma análise detalhada das configurações investigadas, incluindo o modelo do sistema, princípios de operação, estratégia de modulação PWM (do inglês, *Pulse Width Modulation*) e estratégia de controle. A validação das configurações estudadas de forma a verificar a viabiliade, foram realizadas por meio de simulações numéricas e resultados experimentais. Adicionalmente, foram feitas análises comparativas em relação as configurações convencionais e pôde-se verificar benefícios em termos de distorção harmônica e perdas nos dispositivos semicondutores, sobretudo, em cenários de tensão elevada e baixa corrente. As configurações propostas podem ser utilizadas como Condicionadores Unificados de Qualidade de Energia (UPQC, do inglês *Unified Power Quality Conditioner*).

Palavras-chave: Conversor Multinível, Link de Alta Frequência, Sistemas UPQC, Qualidade de Energia.

Abstract

In this work, six single-phase and two three-phase ac-dc-ac configurations that can operate with better levels of harmonic distortion and efficiency than conventional solutions within some application scenarios are analyzed. In this context, this work had the following objectives: *i)* to propose and analyze ac-dc-ac configurations with multilevel characteristics, that is, that can synthesize multilevel waveforms and lower blocking voltages in semiconductor devices; *ii)* to propose and analyze single-phase ac-dc-ac configurations, as well as control strategies that improve the performance of the structure in terms of minimum dc-link voltage and series compensation; *iii)* to propose and analyze three-phase four wire multilevel ac-dc-ac configurations that achieve better performance in terms of minimum dc-link voltage when operating with severely unbalanced loads. The analyzed single-phase and three-phase converters are able to provide a load voltage with constant amplitude and frequency, as well as a sinusoidal grid current with low harmonic content and a high power factor. Furthermore, the studied converters can be used to compensate for harmonics, swells, and sags in the grid voltage, as well as to compensate reactive power and reduce harmonics caused by nonlinear loads. The study methodology for these configurations involves a detailed analysis of the proposed configurations, including the system model, operating principles, PWM modulation strategy, and control strategy. The validation of the studied configurations, to verify their feasibility, was conducted through numerical simulations and experimental results. Additionally, comparative analyses were performed against conventional configurations, demonstrating benefits in terms of harmonic distortion and losses in semiconductor devices, particularly in scenarios of high voltage and low current. The studied configurations can be used as Unified Power Quality Conditioners (UPQC).

Keywords: Multilevel Converter, High-Frequency Link, UPQC System, Power Quality.

List of Tables

List of Figures

List of Symbols

Chapter 2

e_g, e_l	Grid and load voltages.
i_g, i_l	Grid and load currents.
i_s	Shunt compensation current.
I_g, I_l	Amplitude of the grid and load currents.
I_s	Amplitude of the shunt compensation current.
Z_g, Z_l	Grid and load impedance.
L_g, L_l	Grid and load inductors.
v_g	Shunt converter voltage.
v_l	Series converter voltage.
θ_{lg}	Phase angle between v_g and v_l.
E_a	Three-leg dc-link voltage.
E_b	Full-bridge dc-link voltage.
η	Transformer turn ratio.
v_{x0_a}	Pole voltages of the three-leg module with $x \in \{g, l, s\}$.
v_{y0_b}	Pole voltages of the full-bridge module with $y \in \{sa, sb\}$.
$\mathbf{v}$	Voltage vector.
$\mathbf{v}_x, \mathbf{v}_y, \mathbf{v}_z$	The three nearest vectors.
τ_x, τ_y, τ_z	Duty cycles of the three nearest vectors.
P_{in}, P_{out}	Input and output power.
P_{Ca}	Power in the dc-link of the three-leg module.
P_{Cb}	Power in the dc-link of the full-bridge module.
η_p, η_s	Number of turns required by the primary and secondary sides.
v_{pT}	Square-wave voltage in the primary side of the transformer.
ϕ	Triangular magnetic flux.
A	Core area.
$B_{\max}$	Flux density.
*	Asterisk denoting reference values.

Chapter 3

e_g, e_l	Grid and load voltages.
i_g, i_l	Grid and load currents.
i_s	Shunt compensation current.
I_g, I_l	Amplitude of the grid and load currents.
I_s	Amplitude of the shunt compensation current.
Z_g, Z_l	Grid and load impedance.
L_g, L_l	Grid and load inductors.
v_g	Shunt converter voltage.
v_l	Series converter voltage.
η	Turn ratio of the transformer.
η_p, η_s	Number of turns required by the primary and secondary sides.
ϵ	Phase angle between v_g and v_l.
ϕ_g	Phase angle of v_g.
δ_g	Phase angle of e_g.
δ_l	Phase angle between v_g and v_l.
C_a, C_b	Dc links.
E_a	Dc-link voltage A.
E_b	Dc-link voltage B.
η	Transformer turn ratio.
v_{j0m}, v_{0a0b}	Pole voltages of the converter with $j \in \{g1, g2, l\}$ and with $m \in \{a, b\}$.
$\mathbf{v}_{n_a n_b}$	Voltage vector.
$\mathbf{v}_a, \mathbf{v}_b, \mathbf{v}_c$	The three nearest vectors.
τ_a, τ_b, τ_c	Duty cycles of the three nearest vectors.
K	Sectors of the space-vector plane.
p_{Ca}	Power in the dc-link A.
p_{Cb}	Power in the dc-link B.
p_{in}	Input power.
p_{out}	Output power.
i_{Ca}	Current through the dc-link A.
i_{Cb}	Current through the dc-link B.
*	Asterisk denoting reference values.

Chapter 4 - 3LS-UPQC

e_g, e_l	Grid and load voltages.
i_g, i_l	Grid and load currents.
i_s	Shunt compensation current.
I_g, I_l	Amplitude of the grid and load currents.
I_s	Amplitude of the shunt compensation current.
L_s, L_f, C_f	Inductor and capacitors filters.
v_{gs}	Shunt converter voltage.
v_{gl}	Series converter voltage.
v_{Cf}	Output filter voltage.
v_l	Converter output voltage.
q_x	Bidirectional switch.
C	Dc link.
E	Dc-link voltage of the three-leg module.
v_{j0}	Pole voltages of the three-leg module with $j \in \{g, s, l\}$.
$\mathbf{v}$	Voltage vector.
$\mathbf{v}_a, \mathbf{v}_b, \mathbf{v}_c$	The three nearest vectors.
τ_a, τ_b, τ_c	Duty cycles of the three nearest vectors.
T	Sampling period.
K	Sectors of the space-vector plane.
PF_l	Load power factor.
v_μ	Auxiliary variable.
*	Asterisk denoting reference values.

Chapter 4 - SB-3LS-UPQC

L_a, L_l, C_l	Inductor and capacitors filters.
v_{se_s}	Series converter voltage of the two-leg module.
v_{sh}	Shunt converter voltage.
v_{se}	Series converter voltage of the three-leg module.
v_{Cf}	Output filter voltage.
e'_g	Input voltage of the three-leg module.
C, C_s	Dc links of the three-leg and two-leg modules.
E, E_s	Dc-link voltage of the three-leg module and two-leg modules.
v_{j0}, v_{j0_s}	Pole voltages of the three-leg and two-leg modules.
u_b, l_b	Upper and lower hysteresis bands.

Chapter 4 - 3LS-SH-UPQC

i_h	Shunt compensation current of the two-leg module.
L_s, L_f, C_f	Inductor and capacitors filters.
v_{sh}	Shunt converter voltage.
v_{se}	Series converter voltage.
v_{Cf}	Output filter voltage.
v_l	Converter output voltage.
q_x	Bidirectional switch.
C, C_h	Dc link of the three-leg module and hybrid shunt module.
E, E_h	Dc-link voltage of the three-leg module and hybrid shunt module.
v_{j0}, v_{hn0_h}	Pole voltages of the three-leg module and hybrid shunt module.
$\mathbf{v}_{k_x k_y k_z}$	Voltage vector.
$\mathbf{v}_x, \mathbf{v}_y, \mathbf{v}_z$	The three nearest vectors.
τ_x, τ_y, τ_z	Duty cycles of the three nearest vectors.
T	Sampling period.
K	Sectors of the space-vector plane.
PF_l	Load power factor.
v_μ	Auxiliary variable.

Chapter 5

e_g, e_l	Grid and load voltages.
i_g, i_l	Grid and load currents.
i_h	Shunt compensation current.
I_g, I_l	Amplitude of the grid and load currents.
Z_{sh}, Z_{se}	Grid and load impedance.
L_{sh}, L_{se}, C_{se}	Inductor and capacitors filters.
v_{sh}	Shunt converter voltage.
v_{se}	Series converter voltage.
v_l	Converter output voltage.
θ_g	Phase angle of the grid voltage.
C	Dc link.
E_a, E_b	Dc-link voltages.
v_{kj0j}	Pole voltages of the three-leg module and hybrid shunt module.
$v_\mu, v_{\mu_h}, v_{\mu_g}$	Auxiliary variables.

Chapter 6

e_{gj}	Grid voltages.
e_{lj}	Load voltages.
i_{gj}	Grid currents.
i_{lj}	Load currents.
i_{sj}	Shared-leg currents.
i_{fj}	Nine-leg output currents.
i_{hj}	Shunt compensation currents.
I_g, I_l	Amplitude of the grid and load currents.
Z_g, Z_l	Grid and load impedance.
Z_h	Impedance of the shunt converter.
L_g, L_l, C_l	Inductor and capacitors filters.
v_{gj}	Converter voltages at grid side.
v_{lj}	Converter voltages at load side.
v_{rj}	Per-phase converter resultant pole voltages.
v_{gs}	Common mode voltage.
θ_g	Phase angle of the grid voltage.
C	Dc link.
E_j	Dc-link voltages of the nine-leg converter.
E_h	Dc-link voltage of the shunt converter.
$v_{gj0j}, v_{lj0j}, v_{sj0j}$	Pole voltages of the nine-leg converter.
v_{hj0h}, v_{l0h}	Pole voltages of the shunt converter.
$\mathbf{v}_j^*$	Voltage vector.
$\mathbf{v}_{aj}, \mathbf{v}_{bj}, \mathbf{v}_{aj}$	The three nearest vectors.
$\mathbf{v}_{arj}, \mathbf{v}_{brj}, \mathbf{v}_{arj}$	The three nearest vectors in real axis.
$\mathbf{v}_{alj}, \mathbf{v}_{blj}, \mathbf{v}_{alj}$	The three nearest vectors in imaginary axis.
t_{aj}, t_{bj}, t_{cj}	Duty cycles of the three nearest vectors.
T	Sampling period.
K	Sectors of the space-vector plane.
p_{3L_j}	Instantaneous power in each three-leg converter.
p_{gs}	Instantaneous common-mode power.
μ^*	General apportioning factor

Chapter 7

e_{gj}	Grid voltages.
e_{lj}	Load voltages.
i_{gj}	Grid currents.
i_{lj}	Load currents.
i_{sj}	Shared-leg currents.
i_{l0}	Load neutral current.
I_g, I_l	Amplitude of the grid and load currents.
L_g, L_l, C_l	Inductor and capacitors filters.
v_{gj}	Converter voltages at grid side.
v_{lj}	Converter voltages at load side.
v_{rj}	Per-phase converter resultant pole voltages.
v_{gs}	Common mode voltage.
v_{tj}	Voltage in the terminals of the high-frequency transformer.
C	Dc link.
i_{Cj}	Currents in each dc link.
i_{tj}	Currents in the high-frequency transformer.
v_Cj	Dc-link voltages of the nine-leg converter.
v_{aj0}	Pole voltages of the nine-leg converter.
T	Sampling period.
d^*_{aj}	Duty-cycles.
K	Sectors of the space-vector plane.
μ^*	General apportioning factor

Contents

Chapter 1

Introduction

1.1 Presentation of the Theme

In recent decades, due to the expansion of energy demand from residential, commercial, and industrial customers, issues related to the Power Quality (PQ) have become more frequent and critical (KHADKIKAR, 2012; LENG et al., 2016; CARLOS; JACOBINA, 2017). The widespread use of electronic equipment increased the number of disturbances in the electrical grid, such as voltages sags and swells, harmonic content in voltages and currents, voltage fluctuations, interruptions, etc. In the context of power electronics and intending to achieve a scenario with better PQ, equipment such as dynamic voltage restorers (DVR) (MUSARRAT et al., 2023; REDDY; GANAPATHY; MANIKANDAN, 2022; AL-GAHTANI et al., 2022), shunt active power filters (SAPF) (SHUAI et al., 2009; LIU et al., 2019), uninterruptible power supplies (UPS) (WANG et al., 2023a; LOPES et al., 2021), unified power quality conditioners (UPQC) (MONTEIRO et al., 2024; JIA et al., 2023), among others, have become targets of several studies in the technical literature. Devices such as DVRs and series active power filters are used to mitigate disturbances in the grid voltage, such as swells, sags, and harmonic distortions. Shunt active power filters are commonly used to compensate for harmonics and reactive currents from the load. Compared to the devices mentioned above, UPS and UPQC systems achieve prominence due their capability to simultaneously deal with disturbances related to load currents and grid voltages.

The UPS systems generally guarantee uninterrupted voltage supply to sensitive loads such as data centers, telecommunications systems, medical equipment, etc. In addition, if considered in the project, these devices can also compensate for reactive currents and load harmonics, contributing to a low harmonic distortion in the currents from the grid and a high power factor (COSTA et al., 2021). It is worth mentioning that UPS systems

guarantee uninterrupted power supply due to a battery bank connected to the dc link. Conventional UPQC systems are defined in the literature by associating a series and a shunt active power filter, without necessarily using external dc sources. In this way, these devices are commonly used to compensate disturbances from the electrical grid: swell and sags, harmonic and reactive currents, and unbalances. In both UPS and UPQC systems, it is common to use ac-dc-ac converters.

The conventional solution for ac-dc-ac converters, also known as *back-to-back*, has two stages of conversion: the first is responsible for rectifying the ac waveform coming from the power grid, feeding a dc link, and the second by inverting this signal, providing an ac signal to the load. In the two conversion stages, switched circuits with two-level legs are used. In voltage source converters (VSC), the dc link is capacitive and behaves like a voltage source. The current source converters (CSC) (ANTUNES; BRAGA; BARBI, 1999; DING; QUAN; LI, 2018) have inductive dc links that behave as current sources. Other types of converters commonly studied in the technical literature, called impedance source converters (ZSC, *z-source converter*) (PENG, 2003) and matrix converters (NEFT; SCHAUDER, 1992; RAMALHO et al., 2022) can also be highlighted.

To further improve PQ, the focus is also on multilevel converters, as they make it possible to reduce the harmonic distortion of the processed voltages and currents, the reverse voltage in semiconductor devices, power losses, and electromagnetic interference (EMI) (LACERDA; JACOBINA; FABRICIO, 2022). In addition, the weight and volume of the passive filters at the input and output can be reduced. In this context, multilevel topologies are becoming increasingly popular. They can be found in renewable energy applications (wind, solar) and, especially, in various industrial, residential, aerospace, and military environments (VERMA et al., 2023).

In this context, in recent decades, researchers have proposed solutions for more efficient converters, either through the use of new structures or through improvements in the control of conventional configurations. Therefore, this work proposes ac-dc-ac topologies of the voltage source type, focusing on UPQC applications. Single-phase and three-phase ac-dc-ac configurations that can operate with improved PQ are proposed and analyzed. This study involves theoretical analysis, deduction of essential mathematical equations of the converter, numerical simulations, and validation through experimental results.

1.2 Types of Disturbances and Mitigation Alternatives

Maintaining consistent PQ – voltage, current, and frequency stability – is a significant concern for electric utilities, industrial facilities, and end users. This concern has increased as modern appliances have become more sensitive to even minor fluctuations

in the power supply. Historically, power disturbances have been described using different terms, leading to confusion and hindering effective communication. To address this problem, the IEEE standard 1159-1995, "IEEE Recommended Practice for Monitoring Electrical Power Quality," has introduced a standard that defines different PQ issues. In this way, the aim of this section is to present some disturbance found in national and international literature related to PQ, which are used in this work to perform the simulation and experimental tests to verify the feasibility of the proposed configurations. In addition, a brief discussion about the alternatives to mitigate the PQ issues are presented.

1.2.1 Amplitude Disturbances

One can highlight four PQ issues associated with disturbances in the grid voltage at the line frequency: Voltage sag, undervoltage, swell, and overvoltage. Voltage sags and undervoltages are characterized by a reduction in the fundamental frequency of the ac voltage. The key difference lies in how long the disturbance lasts. A voltage sag is a short event lasting between half a cycle and one minute, while an undervoltage lasts longer than one minute. An increase in the fundamental frequency of the ac voltage, on the other hand, characterizes swells and overvoltages. Similarly, a voltage swell is a short event lasting between half a cycle and one minute, while an overvoltage lasts longer than one minute.

The Brazilian reference approved by ANEEL - Procedimentos de Distribuição de Energia Elétrica no Sistema Elétrico Nacional (PRODIST), Módulo 8 – Qualidade de Energia Elétrica - regarding the quality of electrical energy classifies short-term voltage variations (sag and swell) as momentary and temporary, as shown in Table 1.1. As for IEEE 1159 classifies the short-term event regarding duration as being: instantaneous, momentary or temporary, as illustrated in Table 1.2.

Table 1.1 – Classification of short-term voltage variations according to ANEEL - Procedimentos de Distribuição de Energia Elétrica no Sistema Elétrico Nacional (PRODIST), Módulo 8 – Qualidade de Energia Elétrica..

Classification		Magnitude (k)	Duration (t)
Momentary	Sag	0.1 pu $\leq k <$ 0.9 pu	1 cycle $< t \leq$ 3 s
	Swell	$k >$1.1pu	
Temporary	Sag	0.1 pu $\leq k <$ 0.9 pu	3 s $< t \leq$ 60 s
	Swell	$k >$1.1pu	

Typically, series active power filters (SAPF), or DVRs, are used to eliminate grid voltage disturbances. As shown in Fig. 1.1(a), these devices are connected in series with the grid and the load. When a grid voltage transient such as sag or swell occurs, the DVR injects a compensating voltage (v_{se}) to regulate the voltage level throughout the event. This feature enables the protection of critical or sensitive loads. Different types

Table 1.2 – Classification of short-term voltage variations according to IEEE 1159-1995 - "IEEE Recommended Practice for Monitoring Electrical Power Quality".

Classification		Magnitude (k)	Duration (t)
Instantaneous	Sag	$0.1 \text{ pu} \leq k < 0.9 \text{ pu}$	$0.5 \text{ cycle} < t \leq 30/60 \text{ s}$
	Swell	$1.1 \text{ pu} < k \leq 1.8 \text{ pu}$	
Momentary	Sag	$0.1 \text{ pu} \leq k < 0.9 \text{ pu}$	$30 \text{ cycles} < t \leq 3 \text{ s}$
	Swell	$1.1 \text{ pu} < k \leq 1.4 \text{ pu}$	
Temporary	Sag	$0.1 \text{ pu} \leq k < 0.9 \text{ pu}$	$3 \text{ s} < t \leq 60 \text{ s}$
	Swell	$1.1 \text{ pu} < k \leq 1.2 \text{ pu}$	

of configurations and control strategies for this purpose are presented in the technical literature, whether for three-phase or single-phase converters.

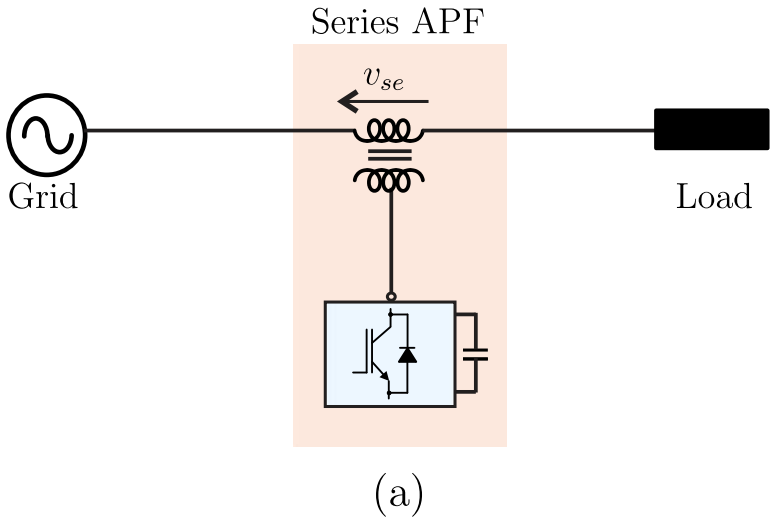
1.2.2 Waveform Distortion

In addition to the disturbances that occur at the amplitude of the fundamental-frequency component, the presence of components in other frequencies consists in a disturbance. These PQ problems can occur in the voltage and current waveforms, are generally not of short duration, and can be classified as harmonics and interharmonics. A harmonic is a component of a periodic wave whose frequency is an integer multiple of the fundamental frequency, while the interharmonics are waveforms with frequency components that are not integer multiples of the frequency at which the system is supplied. Both distortions are usually associated with the increasing operation of static converters, switching power supplies, and other electronic devices. Similar to short- and long-term voltage variations, high levels of harmonics and interharmonics can cause problems in the distribution systems and lead to economic losses due to equipment interruptions in the production line.

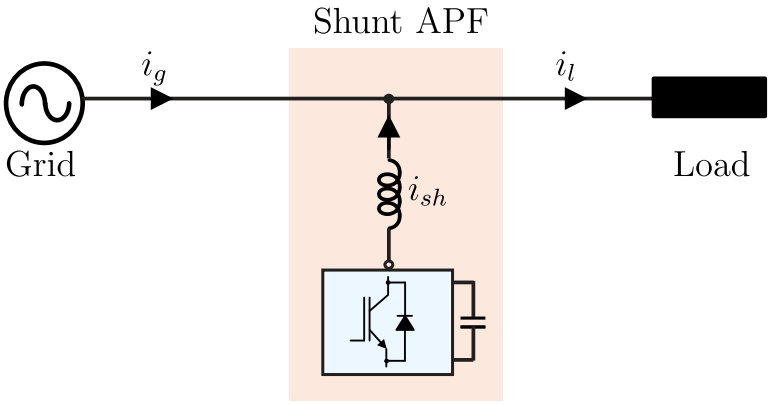
In addition to ensure compensation in the line frequency, the DVRs systems are also able to provided the mitigation of harmonic content in voltage waveforms. On the other hand, to eliminate harmonics in the currents, a shunt active power filter need to be used (SHAPF). Such a device is connected is parallel with grid and load (see Fig. 1.1(b)) and compensate current harmonics by injecting harmonic components (i_{sh}) generated by the load, but in the opposite direction, i.e., phase shifted by 180 degrees.

Since modern power distribution systems typically require better PQ for both voltage and current, installing SAPF and SHAPF together can become less cost-effective. On the other hand, universal active power filter such as UPQC and UPS offer a better solution to improve PQ as the series and shunt compensation structures are usually integrated across a common dc-link (see Fig. 1.1(c)), reducing volume and cost. Better control over the supplied voltage and the consumed current can be achieved simultaneously by using UPQC or UPS.

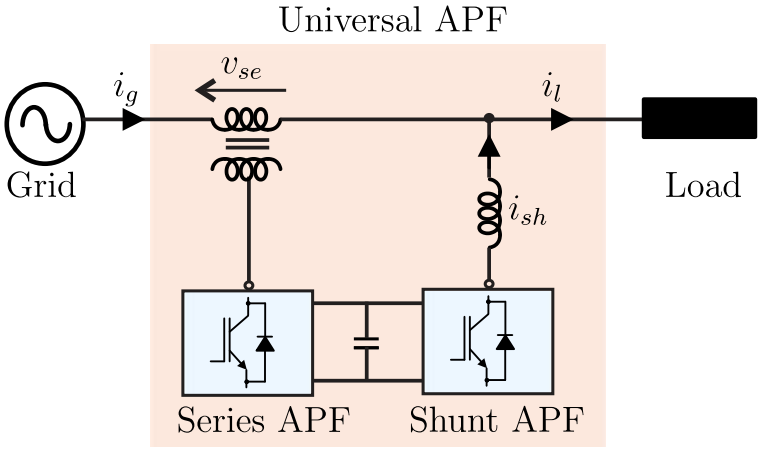
Figure 1.1 – Power quality devices. (a) Series APF. (B) Shunt APF. (c) Universal APF.



(a)



(b)



(c)

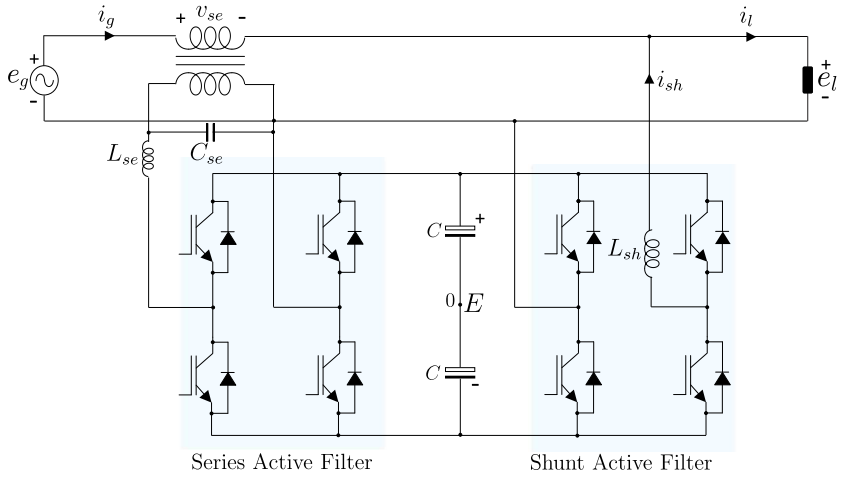
1.3 Bibliographic Review

This section contains a bibliographic review of single-phase and three-phase (four-wire) ac-dc-ac converters that can be used in applications such as UPQC.

1.3.1 AC-DC-AC Single-Phase Converters

As already mentioned, ac-dc-ac converters are often employed for solutions in applications such as UPQC. In Fig. 1.2, it is shown the most conventional configuration used in UPQC applications (MORAN, 1989; KHADKIKAR, 2012; MENG et al., 2022). This configuration comprises two h-bridge inverters, one responsible for compensating disturbances such as harmonics, sags or swells in the grid voltage (series active power filter) and the other for compensating harmonic and reactive currents from the load (shunt active power filter).

Figure 1.2 – Conventional ac-dc-ac converter (MORAN, 1989).



Given the interest in minimizing costs related to power semiconductors, ac-dc-ac configurations were proposed for UPQC applications based on three-leg and half-bridge converters (NASIRI; EMADI, 2003). In Fig. 1.3, the three-leg converter is shown. In this configuration, the common leg share the series and parallel function, generating a coupling in the control of these units and, consequently, generating constraints concerning the phase shift between the voltages generated on the series and shunt side. One can see the half-bridge converter in Fig. 1.4. This structure presents the minimum number of power devices for the operation as ac-dc-ac. However, it needs a voltage at least twice in the dc link compared to the structures with four and three legs and it can not generate multilevel waveforms (PRIETO; SALMERON; HERRERA, 2005). Based on the four- and three-legs structures, other configurations were proposed by changing the position of the low-frequency transformer (LFT) to increase the number of levels generated at the

input and output of the converters (RODRIGUES; JACOBINA, 2018b; HAN et al., 2006; GAUTAM; YADAV; GUPTA, 2012; RODRIGUES; JACOBINA, 2018a; LACERDA et al., 2020).

Still related to cost reduction, single-phase configurations based on the four-leg, three-leg, and half-bridge converter without LFT were proposed since this device is expensive and bulky. In (SANTOS et al., 2014), a transformerless four-leg universal active power filter has been proposed for applications where weight and size are critical factors. This configuration, presented in Fig. 1.5, can compensate for harmonics in the grid voltage and harmonic and reactive currents from the load, guaranteeing unity power factor on the grid side and load voltage with constant amplitude. However, the control of the circulating current is an essential aspect in the design of this converter, as this current can contribute to additional power losses and cause severe instability in the control system, exposing the circuit devices to failure.

Figure 1.3 – Three-leg ac-dc-ac converter (NASIRI; EMADI, 2003).

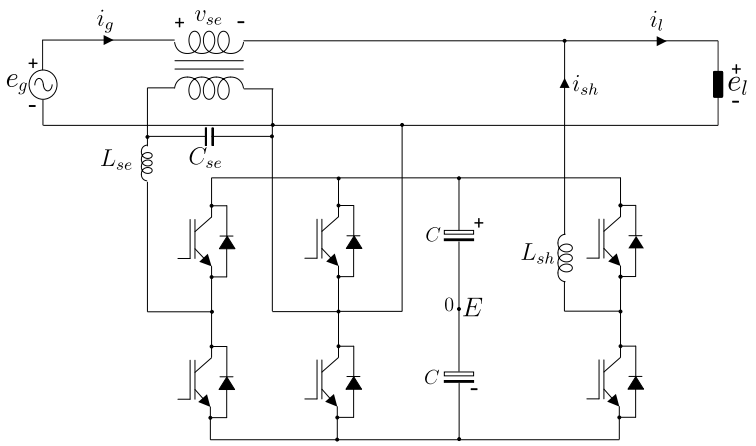


Figure 1.4 – Half-bridge ac-dc-ac converter (NASIRI; EMADI, 2003).

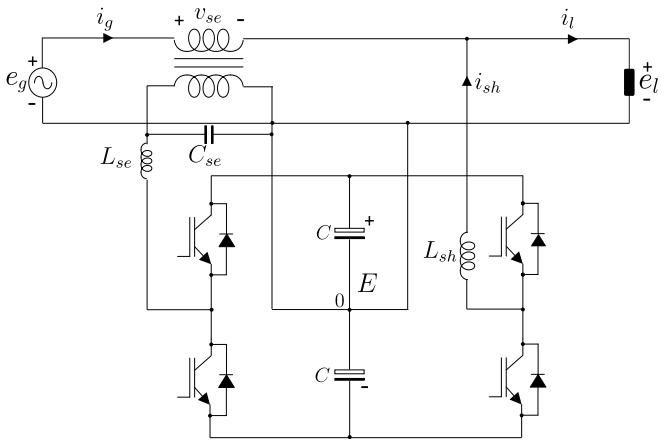
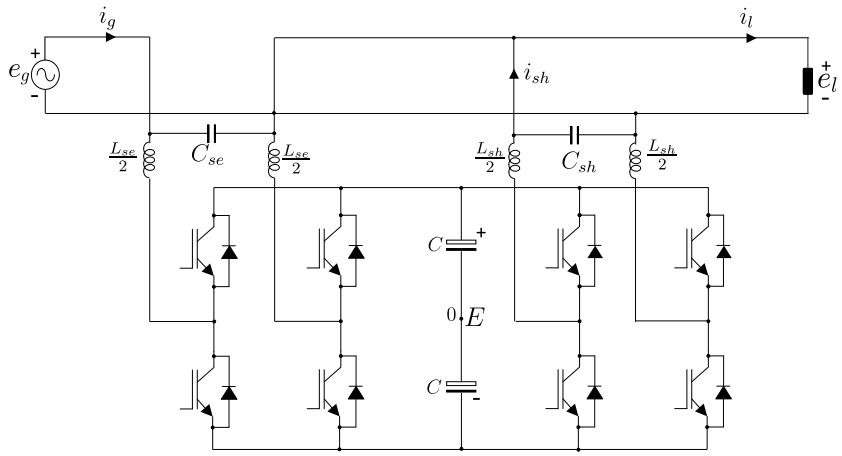
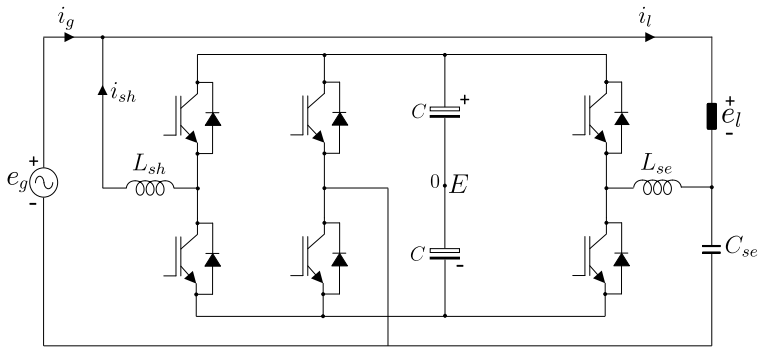


Figure 1.5 – Transformerless four-leg ac-dc-ac converter (SANTOS et al., 2014).



In (LU et al., 2016), a transformerless three-leg converter has been proposed for applications such as UPQC (see 1.6). Furthermore, a control based on space-vector PWM modulation was investigated, which allows optimizing switching losses or harmonic distortion. This configuration performs better when designed to compensate for grid voltage sag disturbances and harmonic and reactive load currents. On the other hand, one of the most critical limitations of the three-leg converter is when it is designed to compensate for voltage swells, since the dc-link voltage must be higher than the amplitude of grid voltage for proper operation. Thus, if the converter is designed to perform such a function, it will operate with a low modulation index on the load side, even under rated conditions, increasing semiconductor power losses and harmonic distortion.

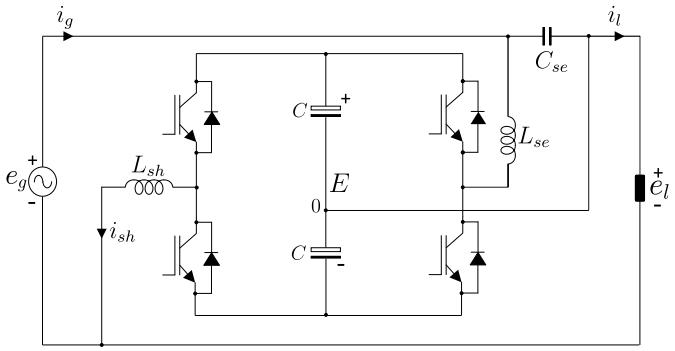
Figure 1.6 – Transformerless three-leg ac-dc-ac converter (3L-UPQC) (LU et al., 2016).



Cheung et al. (2017), Abdalaal e Ho (2022) proposed a transformerless single-phase UPQC based on half-bridge converters, one connected in parallel with the load and the other in series with the grid (see 1.7). Similar to the three-leg converter, this configuration has the capacity for series and parallel compensation. Considering the same conditions, this topology requires twice the dc-link voltage if compared with that of Fig. 1.6 and

can not produce multilevel waveforms. In this context, in terms of cost-effectiveness, a three-leg converter is more suitable, as it reduces the number of power switches compared to a full-bridge converter and presents all switches with half the reverse voltage compared to a half-bridge converter for the same load voltage amplitude.

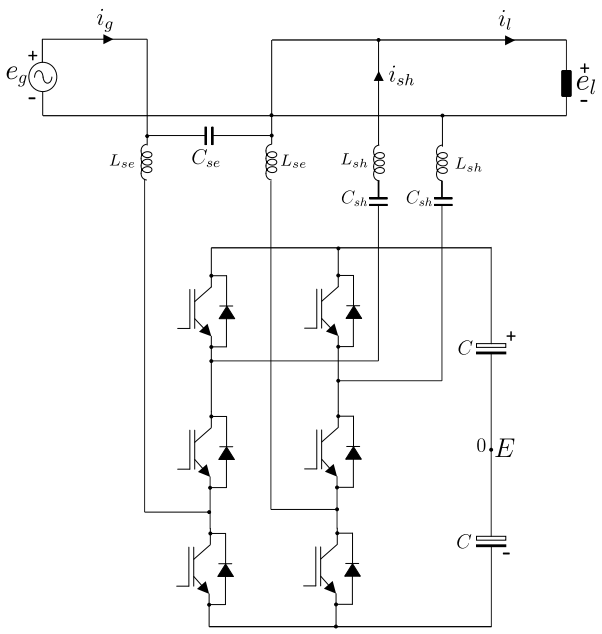
Figure 1.7 – Transformerless half-bridge ac-dc-ac converter (CHEUNG et al., 2017; ABDALAAL; HO, 2022).



An alternative configuration for single-phase transformerless UPQC systems was proposed by Genu et al. (2020). In this solution, there are two sets of single-phase outputs, with each set behaving as an independent converter. The upper unit of the converter is connected in parallel to the load via a series LC filter. It operates as a hybrid power filter, regulating the dc-link voltage and compensating harmonics generated by the nonlinear load. The lower unit operates as a series filter, compensating harmonics, sags, or swells from the grid voltage. It is important to emphasize that using a hybrid power filter enables operation with reduced dc-link voltage and rated power, being an advantage over the topologies already mentioned. On the other hand, similar to (SANTOS et al., 2014), this configuration also has to deal with circulating currents.

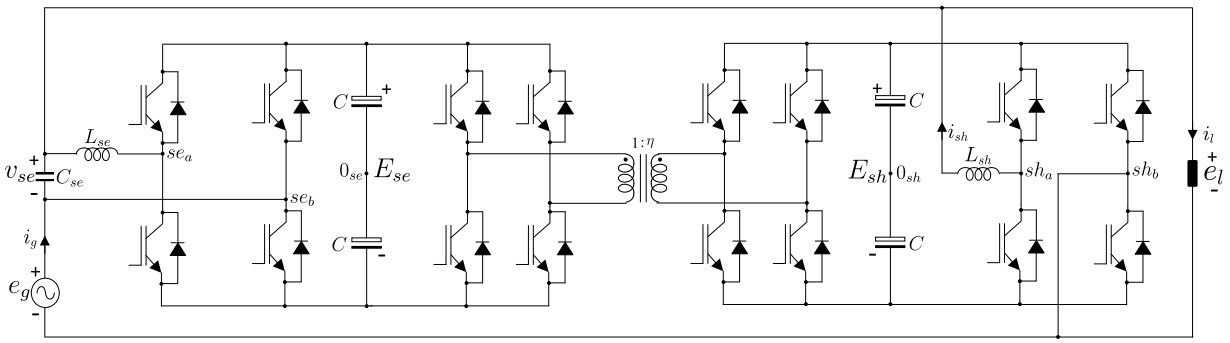
High-frequency transformers (HFT) are another alternative to avoid the problems associated with LFTs. Generally, power electronics solutions based on HFTs reduce size, cost, and losses, allowing operation with minimum voltage on the dc link in voltage source inverters (PEREDA; DIXON, 2011; FILHO et al., 2018; TONGZHEN; JIN, 2014; CARDOSO et al., 2023; KOROGLU et al., 2020; HAN et al., 2021; LACERDA et al., 2023). In (PEREDA; DIXON, 2011), a solution using a high-frequency link (HFL) has been proposed to mitigate the disadvantages of cascaded h-bridge inverters. The HFL allows the use of a single dc source, and the converter generates high voltage levels on the load. For power quality applications such as DVR, (FILHO et al., 2018) proposes a single-phase ac-dc-ac topology with high-frequency isolation. Using the interleaving technique with strongly coupled inductors, this system provides better power loss distribution and reduction of passive filters. In (TONGZHEN; JIN, 2014), a single-phase UPQC that uses an HFL to connect shunt and series units has been investigated. This configuration, shown in Fig.

Figure 1.8 – Transformerless six-switch two-leg converter (GENU et al., 2020).



1.9, can improve system response under grid voltage sags and swells compared to UPQC systems operating without an HFL. In (KOROGLU et al., 2020) and (HAN et al., 2021), three-phase UPQC systems based on HFL were proposed. Due to the high-frequency link, the capabilities of these structures in terms of series compensation have been improved.

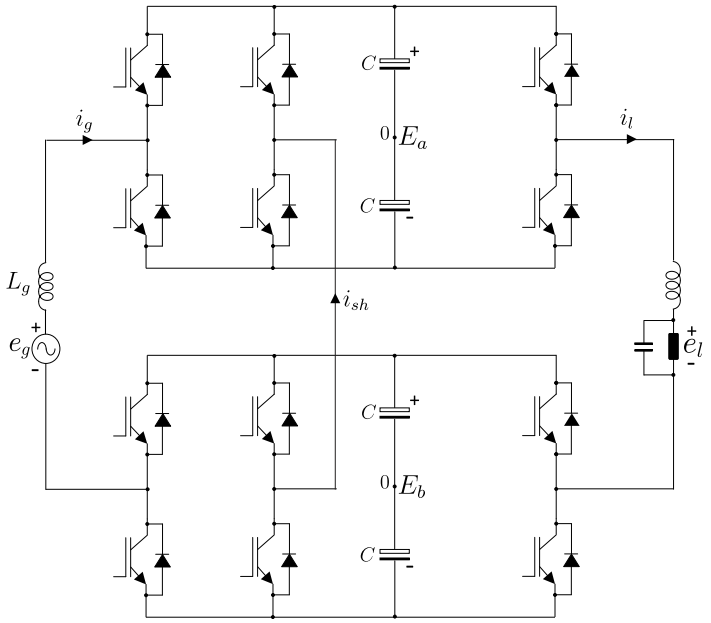
Figure 1.9 – Four-leg single-phase system based on high-frequency transformer (PEREDA; DIXON, 2011).



Additionally, structures based on cascaded three-leg converters and three-leg converters associated with h-bridge structures were also investigated to produce configurations with better performance in terms of harmonic distortion, efficiency, and size of passive filters. In Fig. 1.10, one can observe a configuration associating two three-leg converters, totaling six controlled legs (CHANG; CHANG; CHIANG, 2006). This structure operates with multilevel waveforms. The grid and load sides can reach up to nine voltage levels operating with asymmetric voltages on the dc links. Based on this structure, configurations with a reduced number of active switches were proposed (FREITAS et al., 2018). Compared

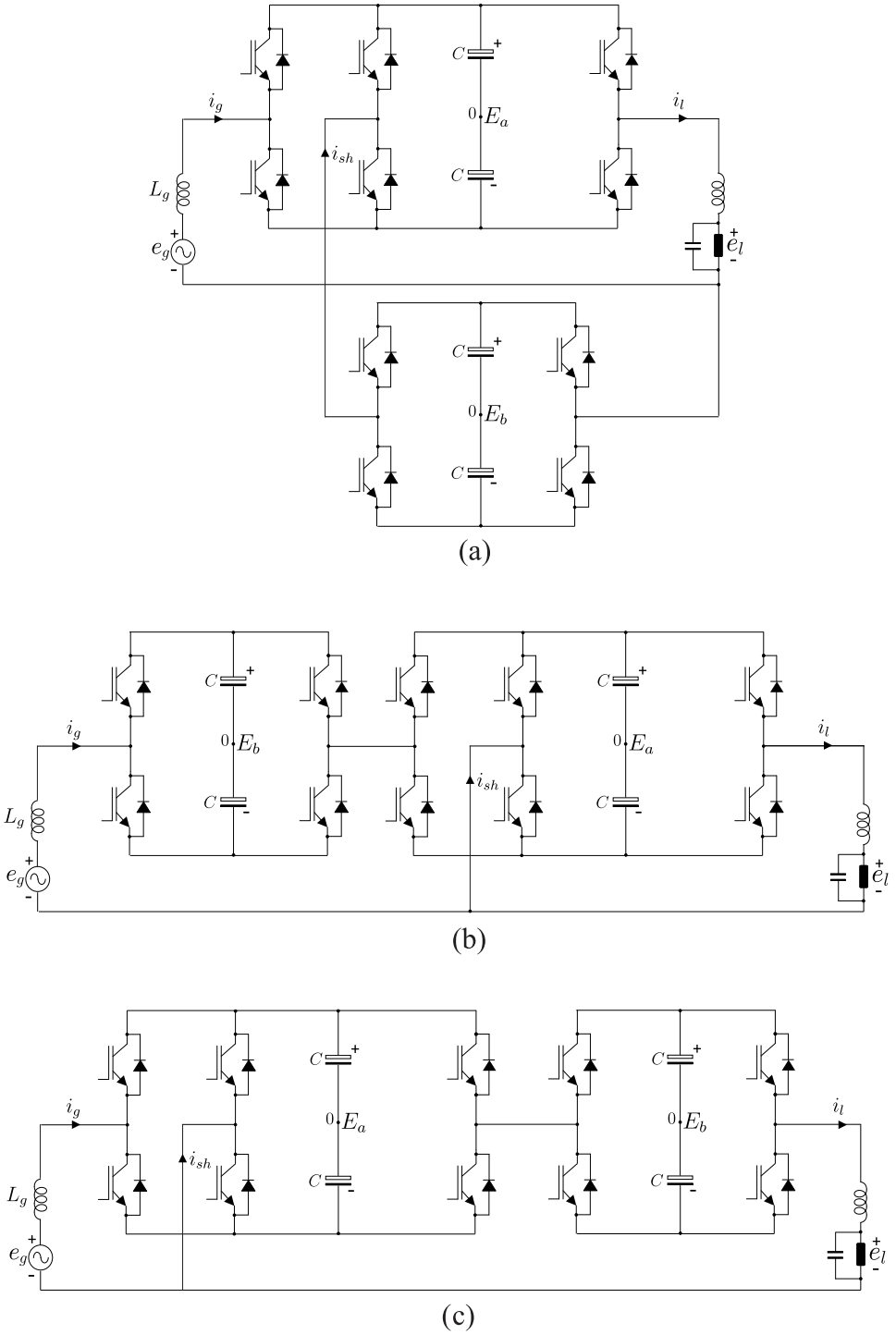
with the conventional structure with six controlled legs, it is possible to reduce the number of drivers and controlled switches, reducing the system's total cost. However, the converter becomes non-regenerative and is only suitable for applications where regenerative operation is impossible or not desired. It is also important to emphasize that using uncontrolled legs results in limitations. It is reported in the technical literature that for correct operation, it is necessary to synchronize the voltage generated at the converter's input with the voltage generated at the output side (COSTA et al., 2021).

Figure 1.10 – Ac-dc-ac six-leg converter (CHANG; CHANG; CHIANG, 2006).



Then, three configurations were proposed associating the three-leg converter in series with an h-bridge converter. In Fig. 1.11, one can observe three different ways of connecting an h-bridge converter to the three-leg configuration: *i)* on the shared leg (MAIA; JACOBINA, 2014), *ii)* on the grid side (MAIA; JACOBINA, 2017), *iii)* on the load side (LACERDA; JACOBINA; FABRICIO, 2022). The first option is suitable for applications where the grid and load voltages are the same in rated conditions. In the second structure, inserting an h-bridge on the load side makes it possible to increase the converter's capacity to compensate for swells. The third option performs best in applications where the load voltage is twice the grid voltage. These three structures can generate multilevel waveforms on the grid and load side, with the first option being the configuration with the best performance in terms of harmonic distortion. It is noteworthy that these topologies make use of more than one dc-link capacitor. Thus, limitations related to a more complex control for voltage balancing and series compensation capability are reported (MAIA; JACOBINA, 2014).

Figure 1.11 – Single-phase ac-dc-ac five-leg converters. (a) Based on three-leg and a h-bridge connected to the common part of the converter (MAIA; JACOBINA, 2014). (b) Based on three-leg and a h-bridge connected in the grid side (MAIA; JACOBINA, 2017). (c) Based on three-leg and a h-bridge connected in the load side (LACERDA; JACOBINA; FABRICIO, 2022).



Another alternative to produce multilevel voltages in ac-dc-ac converters is using multilevel legs, such as neutral-point-clamped (NPC) (LIN; DONG, 2023), flying capacitor (FC) (ELRAIS; SAFAYATULLAH; BATARSEH, 2023), T-type (SHARIDA et al., 2023) and vienna (YIP et al., 2022). Among the single-phase multilevel structures, the three-leg

converter that uses NPC-type legs can be highlighted also as conventional (LIN; LEE; CHEN, 2002; FREITAS et al., 2010). This structure is shown in Fig. 1.12. Using the NPC leg reduces the voltage stresses on the power switches in half regarding the conventional three-leg structure. Furthermore, this topology allows the generation of five voltage levels on the grid and load side. In (KWON; KWON; KWON, 2018), a high-efficiency ac-dc-ac converter has been proposed using SiC mosfests. The converter comprises two T-type legs on the grid and load side and a two-level leg as shared leg (see Fig. 1.13). It is observed that the prototype reached a high efficiency, approximately 99%. Additionally, the converter generates five voltage levels on the grid and load side. Lin e Huang (2004) proposed an ac-dc-ac converter that has in its structure two flying capacitor legs and a two-level leg, as can be seen in the Fig. 1.14. Similar to the previous configurations, this one allows generating five voltage levels on the grid and load side. However, an increase in the number of floating capacitors is reported, which brings more complexity in the control system.

Figure 1.12 – Single-phase ac-dc-ac converter based on NPC leg (FREITAS et al., 2010).

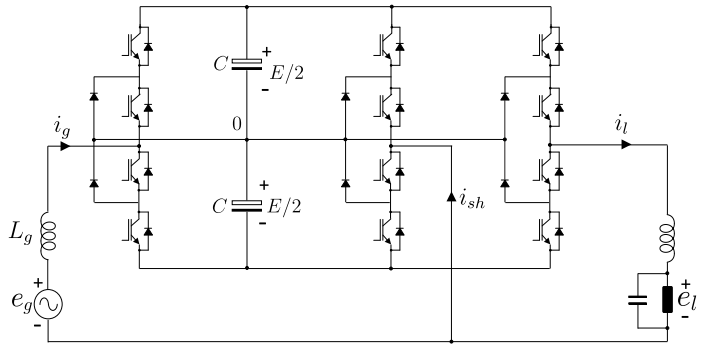
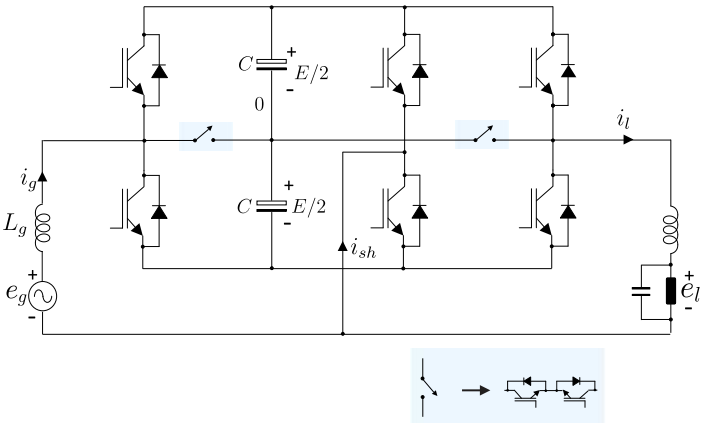
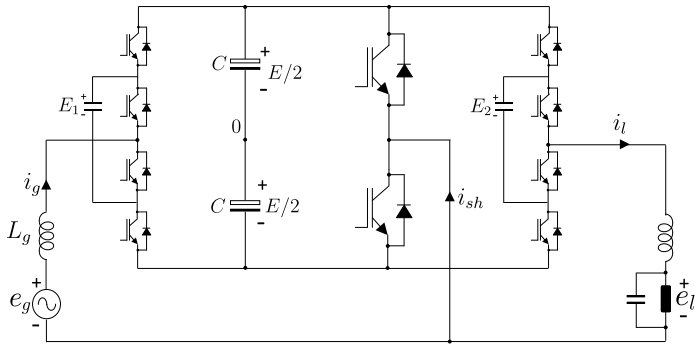


Figure 1.13 – Single-phase ac-dc-ac converter based on t-type leg (KWON; KWON; KWON, 2018).



Multilevel ac-dc-ac converters have become a promising solution for low-power applications due to technical advantages that, although more commonly associated with medium- and high-power systems, can also benefit smaller-scale scenarios. The motivations for using these converters in low-power applications can be understood through the following characteristics:

Figure 1.14 – Single-phase ac-dc-ac converter based on flying capacitor leg (LIN; HUANG, 2004).



- **Power quality:** Power quality can be critical in low-power applications, mainly in sensitive systems such as medical devices, communication systems, and consumer electronics (MICHALEC et al., 2021). Single-phase multilevel converters can generate waveforms with low harmonic content. This generally reduces the need for additional filtering and improves the overall system performance.

- **Efficiency:** Despite their smaller size and capacity, efficiency remains an important criterion in low-power applications, where every watt saved can have a significant impact on operating costs. In this context, multilevel converters can operate with lower switching losses, improving energy efficiency and contributing to more economical operation (KWON; KWON; KWON, 2018).

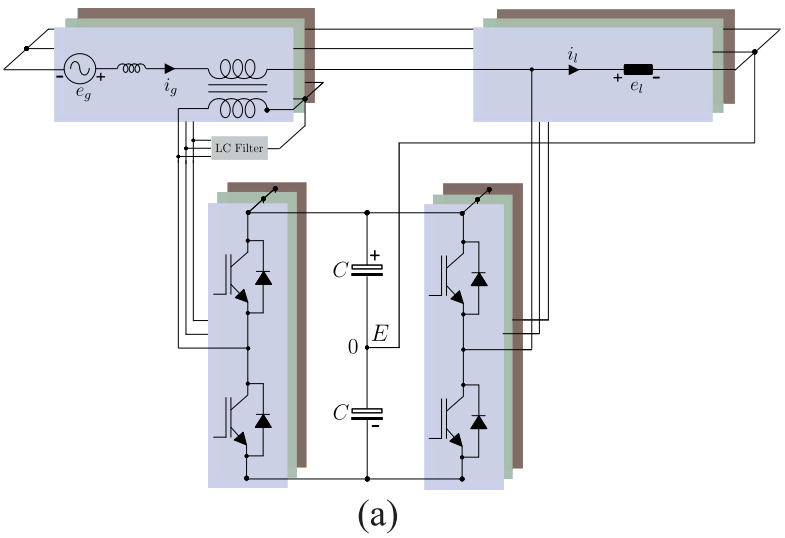
- **Lower rating in the semiconductor devices:** In a multilevel converter, the switches, generally, have lower voltages compared to two-level converters. This is also advantageous in low-power applications, where semiconductors with lower voltage ratings can reduce costs and improve reliability (MAIA; JACOBINA, 2017).

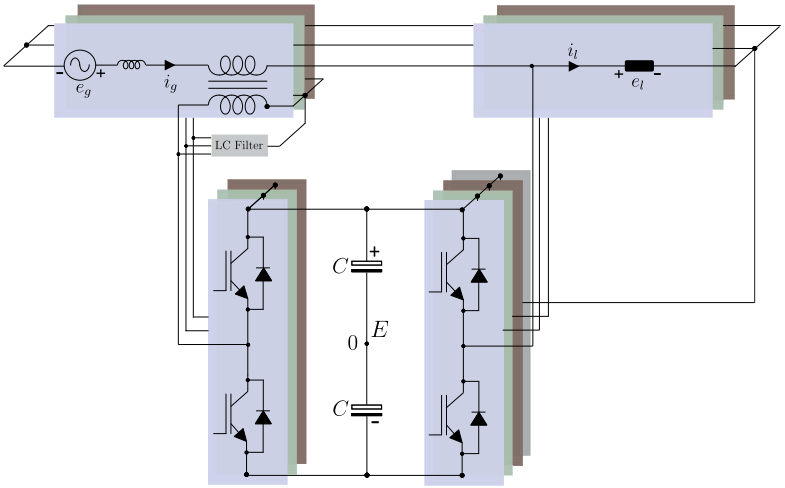
In view of this, in recent years, researchers have aimed to find more and more solutions for multilevel converters to make them more efficient, robust, and with a lower manufacturing cost when compared to conventional solutions. In this way, technological advances have allowed the manufacture of semiconductor devices with better efficiency and reliability. Additionally, in the technical literature, it is possible to observe the association of different types of legs to maximize the voltage levels. Thus, depending on the application and the imposed restrictions, many options exist for generating PQ. Therefore, part of this work addresses new solutions for ac-dc-ac multilevel converters with shared-leg for applications in single-phase UPQC systems. The studied configurations guarantee unity power factor on the grid side and maintenance of the amplitude and frequency of the load voltage.

1.4 AC-DC-AC Three-Phase Four-Wire Converters

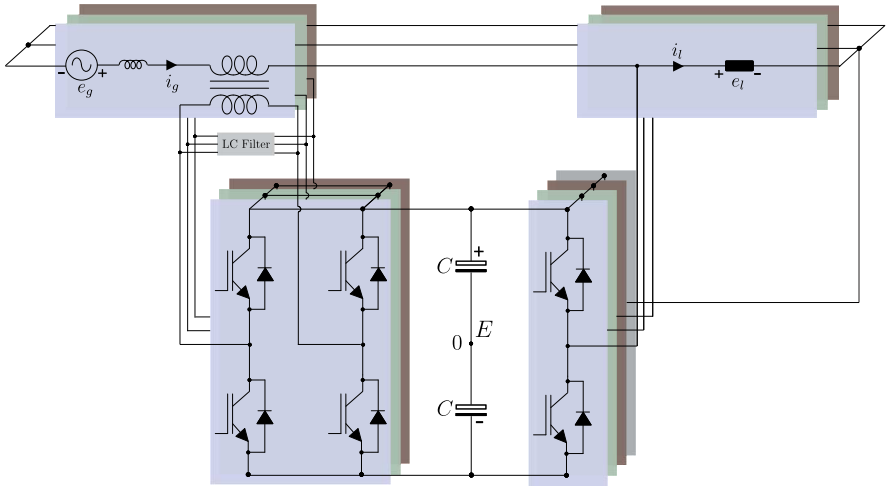
Following the same concept as single-phase converters, three-phase ac-dc-ac structures consist of series and shunt units that are responsible for compensating voltage disturbances from the grid and harmonic and reactive power in the load. In a three-phase four-wire power distribution system that supplies single-phase loads, unbalanced currents often occur. In this context, the shunt unit of the converter is also responsible for compensating these unbalances, ensuring controlled currents in the grid with a high power factor. Figure 1.15 shows the conventional configurations used as UPQC. In Fig. 1.15(a), the series and shunt units consist of three-phase half-bridge converters. In this configuration, the central point of the dc link is used as the connection point for the fourth wire, so additional control is required to balance the voltage of the two individual capacitors. To reduce the complexity of the control strategy and avoid higher voltages on the dc-link, a fourth leg was added to the shunt converter unit to connect the fourth wire (see Fig. 1.15(b)). Another option presented in the technical literature is shown in Fig. 1.15(c). This structure uses h-bridge converters in the series unit to reduce the voltage requirements on the dc-link. However, this configuration increases the number of semiconductor devices, power losses, and the overall size of the system (KHADKIKAR, 2012).

Figure 1.15 – UPQC configurations with low-frequency transformers. (a) UPQC configuration based on six legs with the central point of the dc link used as the connection point for the fourth wire. (b) UPQC configuration based on seven legs. (c) UPQC configuration based on ten legs with h-bridge converters in the series unit.





(b)

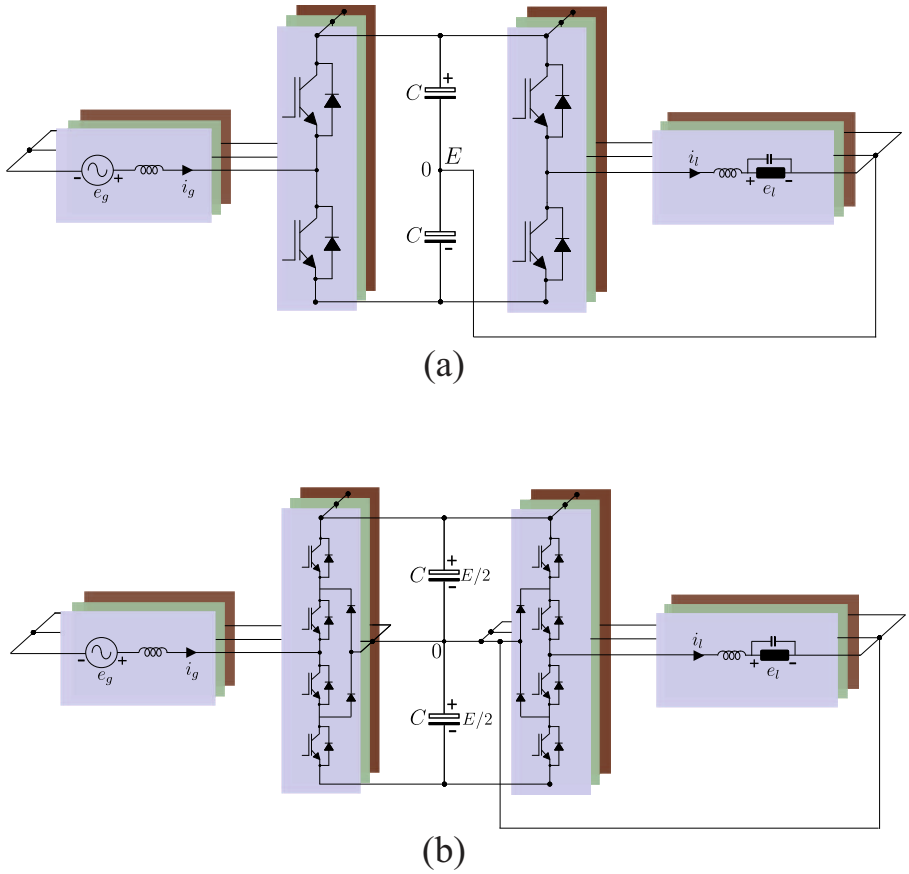


(c)

In order to increase the cost-effectiveness of the system, three-phase configurations that do not use LFTs have also been proposed. In Fig. 1.16(a-b), conventional transformerless topologies employing two-level legs (Fig. 1.16(a)) and three-level legs (Fig. 1.16(b)) can be observed. Although these configurations were proposed in (KIM; KWON; KWON, 2009) and (CASEIRO; MENDES; CRUZ, 2020), respectively, for UPS solutions, they can also be employed in applications such as UPQC. It is worth noting that for the topology presented in Fig. 1.16(a), it is possible to connect the fourth wire to the midpoint of the dc link or add another leg for this connection, thereby avoiding, as already mentioned, increased complexity in the control system (WU et al., 2017).

Other ac-dc-ac configurations have been proposed using four-leg and three-leg converters. In Fig. 1.17(a), a structure composed of a four-leg per phase back-to-back converter can be observed (OLIVEIRA et al., 2020). This structure operates with lower dc-link voltages compared to the configurations presented in Fig. 1.16. On the other hand, the

Figure 1.16 – Three-phase UPQC configurations without low-frequency transformers. (a) UPQC configuration based on six legs with the central point of the dc link used as the connection point for the fourth wire. (b) Multilevel UPQC configuration based on NPC legs.

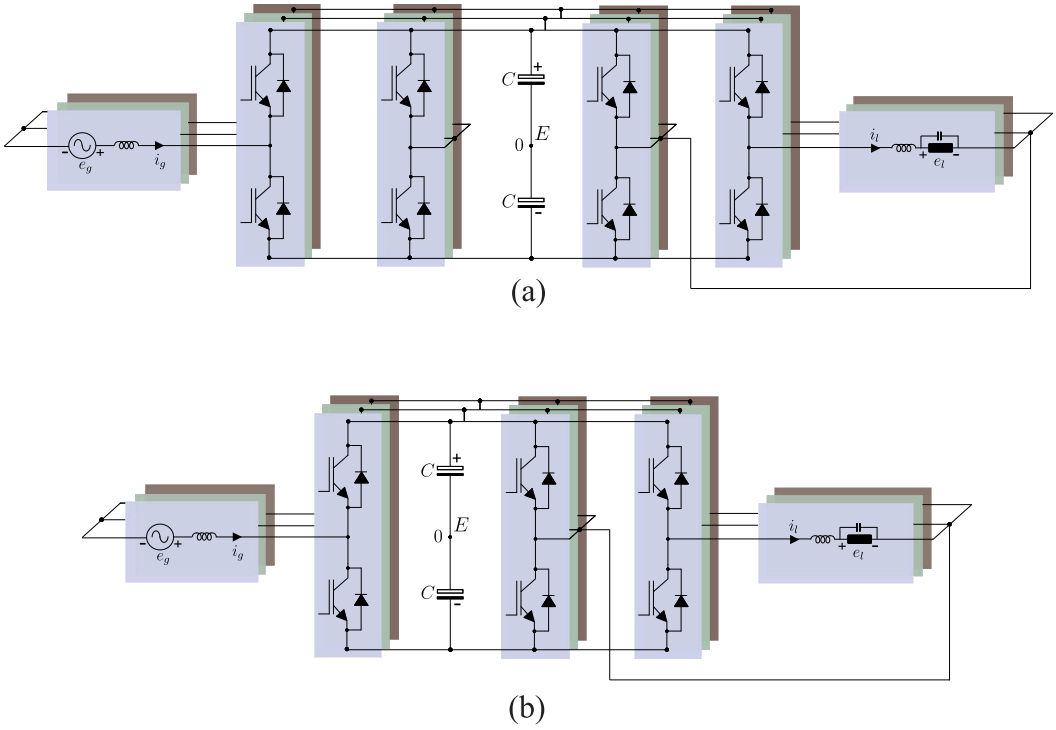


control system for this configuration needs to be designed to mitigate circulating currents. Fig. 1.17(b) presents an alternative to avoid circulating currents. Ac-dc-ac converters with shared legs between the series and shunt units provide a reduction in the number of power semiconductors. They can operate with minimized currents in the shared leg, reducing conduction losses. This configuration operates with minimal dc-link voltages in applications where the input and output operating frequencies are the same, as in UPQC systems. However, this structure presents challenges in controlling the dc-link voltages when operating with unbalanced loads.

Another alternative to avoid LFTs is separating the series and shunt units into modules with individualized dc links, as shown in Fig. 1.18 (VENKATRAMAN; SELVAN, 2017). This structure comprises three half-bridge converters on the series side and a three-phase converter on the shunt side. Given the number of floating capacitors in the structure, it is necessary to use control strategies or fixed dc sources to regulate the dc links. For applications where it is unnecessary to compensate for severe sags and swells, quadrature control is commonly used, allowing the series converters to provide voltages in quadrature with the currents and, thus, eliminating the need for active power flow from

the converter. On the other hand, the level of sag and swell that can be compensated depends on the grid power factor. In general, higher dc-link voltage values are required for the correct operation of the structure. Additionally, this control technique has the disadvantage of load voltage phase jumps at the moment of compensation, which can cause issues to sensitive loads.

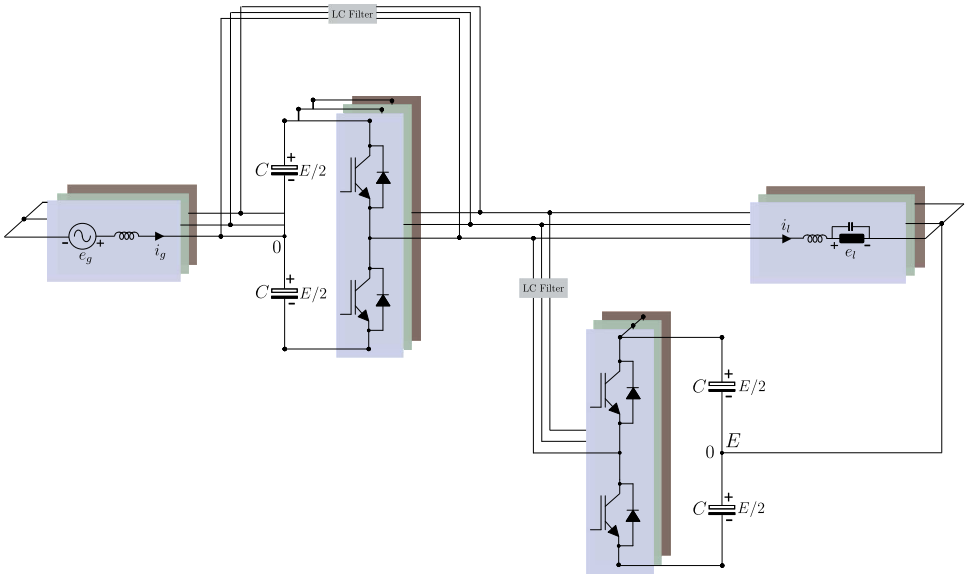
Figure 1.17 – Multilevel three-phase UPQC configurations without low-frequency transformers based on single-phase ac-dc-ac modules. (a) Twelve-leg converter based on a full-bridge module per phase. (b) Nine-leg converter based on a three-leg converter per phase.



In the same perspective, a configuration for applications such as a Unified Power Flow Controller (UPFC) has been proposed in (PENG et al., 2016). Although structurally similar to UPQC devices, UPFCs are generally employed in power transmission systems. In this context, a higher number of power semiconductors is required to withstand the high voltage levels. This configuration consists of cascaded h-bridge converters in the series and shunt units, aiming to achieve high voltage levels without using LFTs. Compared to the conventional one that uses transformers, some advantages mentioned in the technical literature regarding this structure include a highly modular structure, low weight, high efficiency, high reliability, low cost, and fast dynamic response.

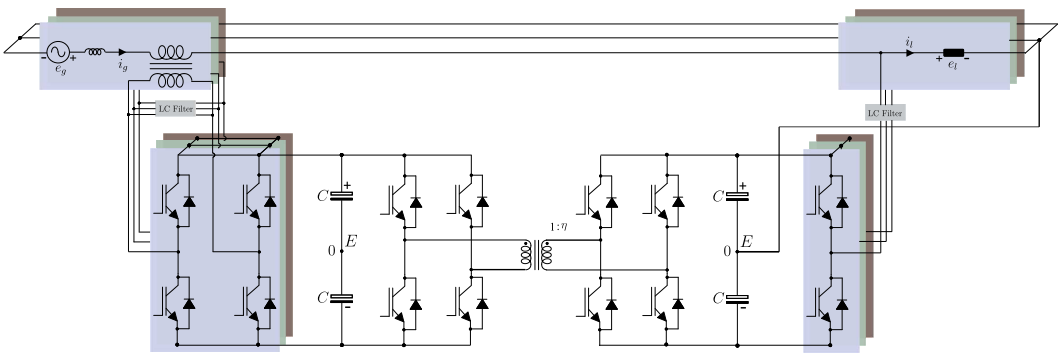
Solutions involving HFLs have also been proposed for three-phase structures. As previously mentioned, systems based on HFLs offer advantages, such as high power density and reduced system cost. UPQCs that operate with HFLs have attractive performance in terms of cost, size, and reduced losses in the semiconductor devices of voltage source converters, as the dc-link voltage can be minimized (CARDOSO et al., 2023). A UPQC

Figure 1.18 – Three-phase UPQC configurations without low-frequency transformers based on separate series and shunt units into modules with individualized dc links.

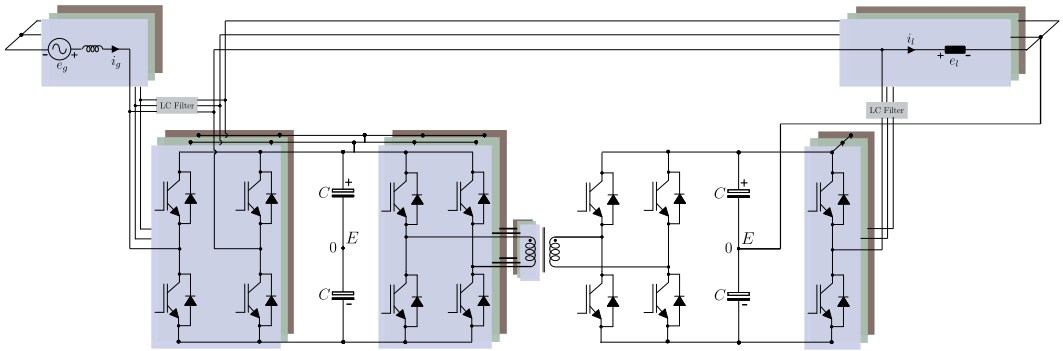


utilizing a bidirectional HFL, which also employs LFTs, was investigated by Koroglu et al. (2020) (Fig. 1.19(a)). In (Savrun et al., 2020) and (HAN et al., 2021), a topology with a bidirectional HFL have been proposed, featuring a three-phase converter in the shunt unit and h-bridge converters in the series unit (Fig. 1.19(b)). In (TONGZHEN; JIN, 2014), a UPQC with a bidirectional HFL has been proposed, utilizing h-bridge modules in both the shunt and series units, as shown in Fig. 1.19(c). To simplify the control of bidirectional HFLs, a structure employing a unidirectional HFL was proposed by Felinto, Cunha e Jacobina (2022). This solution reduces the cost of controlled switches and offers more straightforward control. However, operation during voltage swells is only permitted with the use of a safety resistor to dissipate the excess power absorbed by the dc links.

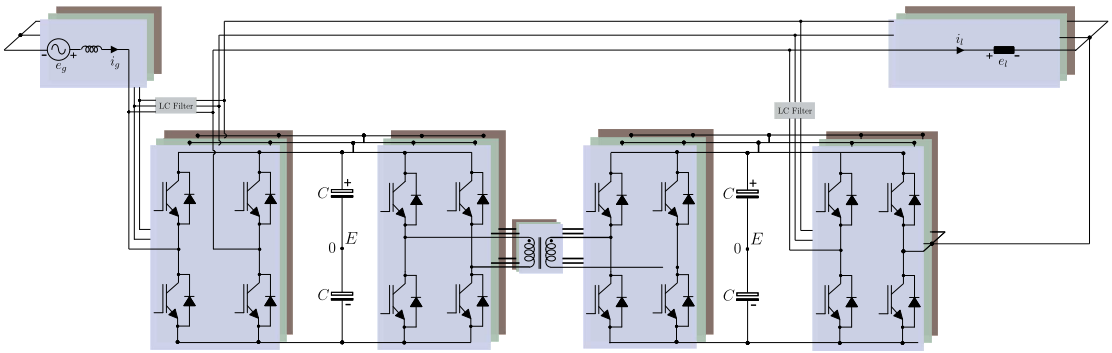
Figure 1.19 – Three-phase UPQC configurations based on high-frequency transformers. (a) Three-phase UPQC configuration with fourteen legs. (b) Three-phase UPQC configuration with eighteen legs. (c) Three-phase UPQC configuration with twenty four legs.



(a)



(b)



(c)

1.5 Objectives

After locating the theme of the research and to present the literature review, the objectives can be defined as:

- Propose and analyze ac-dc-ac single-phase configurations with multilevel characteristics, i.e., that they can synthesize multilevel waveform and reduce voltage ratings in the semiconductor devices;
- Propose and analyze ac-dc-ac single-phase configurations, as well as control strategies, in order to improve the performance of the structure in terms of dc-link voltage level and series compensation capacity;
- Propose and investigate ac-dc-ac three-phase four-wire configurations, as well as control strategies, in order to improve the performance of the structures under severe unbalanced load;
- Bring contributions in PWM modulation and control techniques to obtain optimal solutions for the proposed configurations. This study involves theoretical analysis, numerical simulations, and deduction of mathematical equations of the converters;
- Through numerical simulations, evaluate the operation and performance of the studied structures regarding harmonic distortion and power losses of semiconductor

devices. In addition, present a comparative analysis of the proposed and investigated alternatives with conventional configurations published in the technical literature;

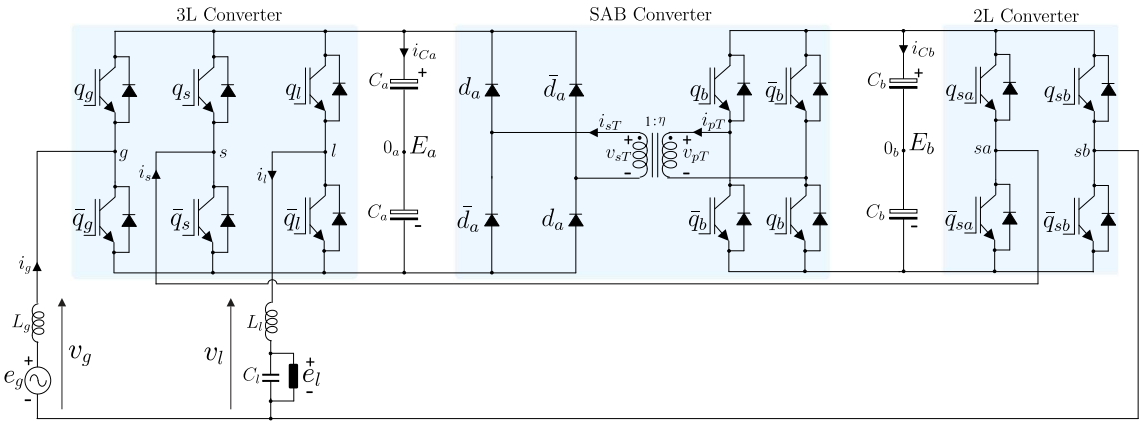
- From experiments carried out in the laboratory, validate the simulation results and verify the viability of the proposed and investigated structures.

1.6 Contributions

In this work, six single-phase ac-dc-ac structures and two three-phase four-wire ac-dc-ac configurations are investigated for application as UPQC. First, two single-phase ac-dc-ac configurations with multilevel characteristics are proposed. Next, four configurations based on three-leg or h-bridge converters, as well as new decoupled method of the series and shunt units are investigated to improve series compensation, harmonic distortion, and efficiency. Lastly, two three-phase four-wire ac-dc-ac structures based on nine-leg converter with the capability of compensate severe unbalanced loads are investigated.

In Chapter 2, it is proposed the configuration shown in Fig. 1.20. This structure comprises modules with two and three legs and a single active bridge based on HFT. Using the HFL, it is possible to improve power quality, increase efficiency, and simplify the control strategy. The proposed topology is analyzed with symmetric and asymmetric voltages on the dc-link, which allows generating input and output waveforms with up to nine levels. Additionally, a comparative study is made regarding harmonic distortion and losses in power semiconductors concerning the conventional topology shown in Fig. 1.9. Simulations and experimental results are presented to confirm the viability of the proposed converter.

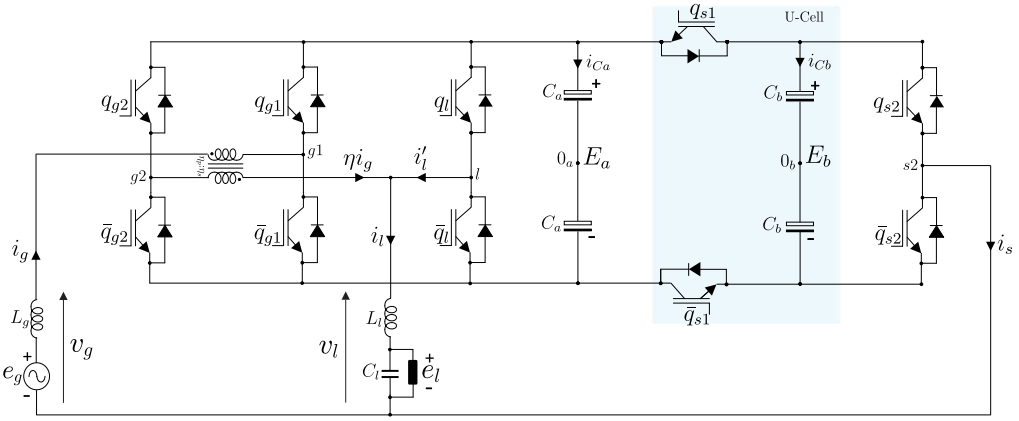
Figure 1.20 – Proposed five-leg ac-dc-ac converter based on high-frequency transformer.



Then, Chapter 3 presents a single-phase ac-dc-ac configuration based on the PUC (*packed u-cell*) inverter. Each U cell consists of two IGBTs and a capacitor, as seen in 1.21. This cell and its association were introduced in (OUNEJJAR; AL-HADDAD; GREGOIRE,

2011) to achieve a multilevel structure with a reduction in the number of power switches, a reduction in the number of capacitors, low harmonic content, and low manufacturing cost. The configuration also uses a LFT, which makes it possible to generate multilevel waveforms at the converter's input and increase the capability to compensate grid voltage swells with minimum voltages on the dc link. Likewise, a comparative study is performed regarding the converter's main characteristics: power processed by the transformer, blocking voltage in semiconductors, average switching frequency, harmonic distortion, and losses in semiconductors. Simulations and experimental results are presented to confirm the viability of the proposed converter.

Figure 1.21 – Proposed ac-dc-ac converter based on PUC converter.



Chapter 4 presents new decoupling methods to improve the performance of single-phase transformerless UPQC based on three- and five-leg converters under grid voltage swells. A reconfiguration of the three-leg module using a bidirectional switch is proposed to improve the voltage swell capability [see Fig. 1.22]. Then, two five-leg configurations are presented, one based on three-leg and shunt modules and another based on three-leg and standby converters [see Figs. 1.23 and 1.24]. The systems studied provide a unity power factor on the grid side with high power quality and feed the load with a sinusoidal waveform during both voltage swell and sag. The system model, dc-link voltage specifications, pulse-width modulation (PWM) techniques, and overall control strategies are presented. Simulation and experimental results are also addressed to evaluate the feasibility of the proposed systems.

Chapter 5 presents a single-phase transformerless UPQC based on two h-bridge modules [see Fig. 1.25]. In the proposed configuration, the way the load is connected allows the natural dc-link voltage balancing, which simplifies the design of the control strategy compared to the conventional transformerless UPQCs. The proposed configuration can compensate for grid voltage disturbances such as grid voltage sag and swells and provide grid power factor correction operating with minimum dc-link voltage values. The system model, operating conditions, overall control system, and a pulse width modulation that

Figure 1.22 – Proposed transformerless three-leg converter.

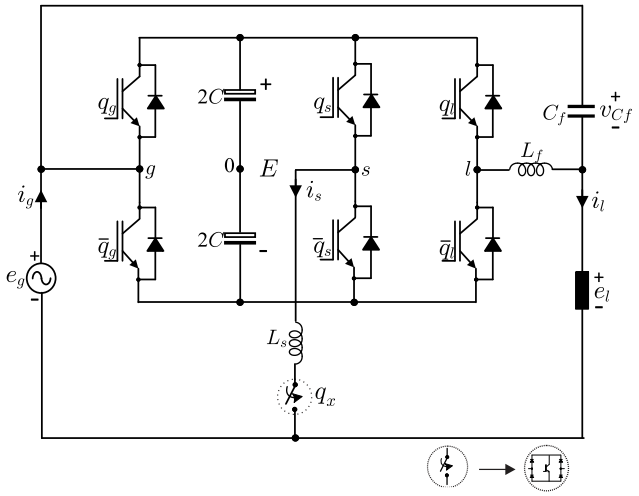


Figure 1.23 – Proposed SB-3LS-UPQC configuration.

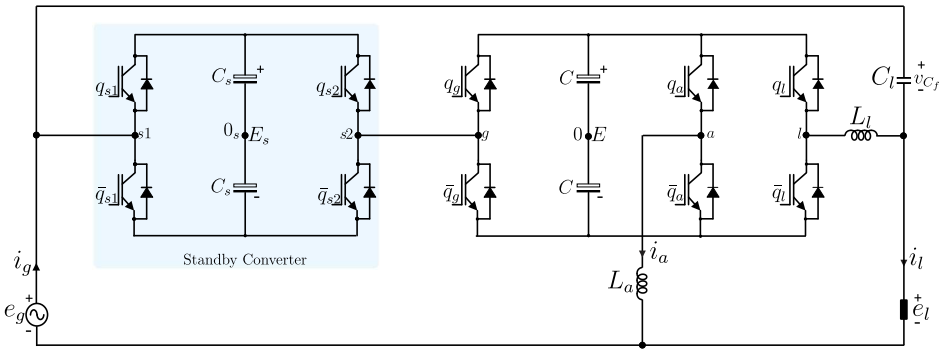
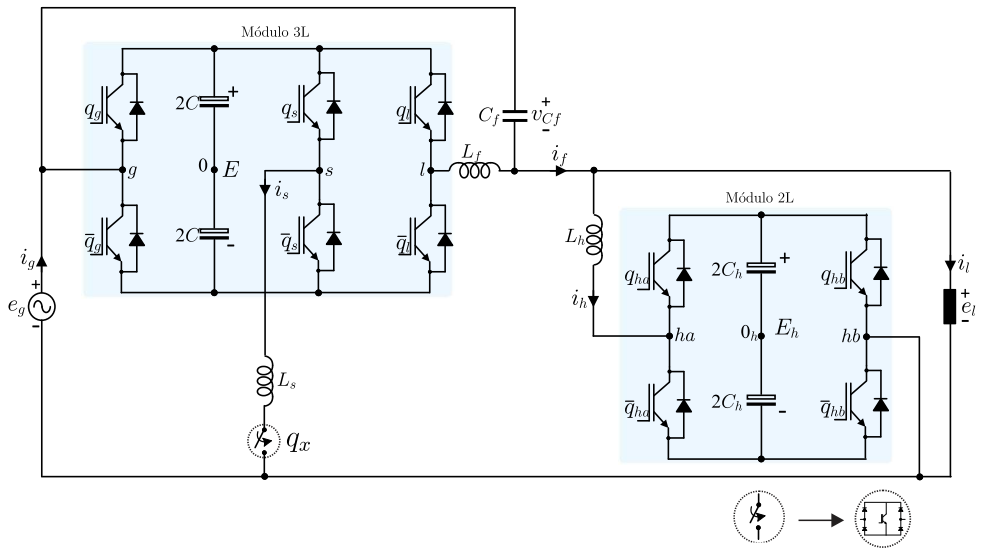
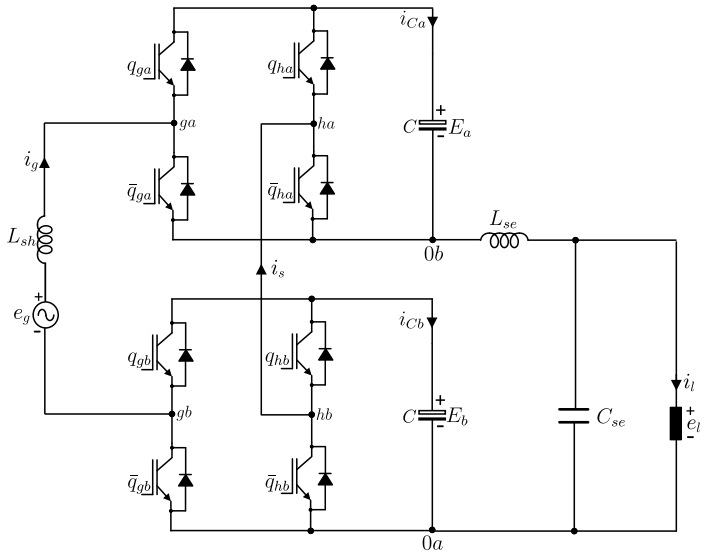


Figure 1.24 – Proposed 3LS-SH-UPQC configuration.



exploits a simplified carrier-based approach are presented. Simulation and experimental results are also presented to evaluate the feasibility of the proposed system.

Figure 1.25 – Proposed 4L-UPQC configuration.



Chapter 6 proposes a three-phase transformerless UPQC based on a nine-leg converter and a four-wire shunt converter [see Fig. 1.26]. The system ensures grid power factor compensation with low harmonic content and feeds the load with a sinusoidal waveform. The shunt converter provides balanced currents, allowing the nine-leg converter to operate with a wide range of unbalanced loads while compensating the harmonic content. In addition, the shared-leg currents are minimized, which reduces power losses. Compared to the conventional transformerless UPQCs, the proposed converter achieved lower total semiconductor losses under a severe unbalanced load. This chapter discusses the system model, pulse-width modulation (PWM) techniques, and control strategy. Simulations and experimental results are presented to confirm the feasibility of the proposed structure and the correctness of the design methodology.

In Chapter 7, the configuration presented in Fig. 1.27 is investigated. This configuration consists of a three-phase four-wire converter composed by a ac-dc-ac three-leg module in each phase and a bidirectional three-port dc-dc converter isolated with a three-winding high-frequency transformer. This connection allows the investigated converter to operate with unbalanced power conditions, because the TAB is able to redistribute power among the converter phases. Converter model is provided, as well as pulse-width modulation, control strategy, and a comparative analysis. Experimental results are presented for validation purposes under severe unbalanced conditions. Compared with conventional solutions, the investigated converter offers advantages such as not requiring LFTs. In addition, compared to solutions that use high-frequency links, it reaches better results in terms of harmonic distortion and power losses.

Figure 1.26 – Proposed 9LS-UPQC configuration.

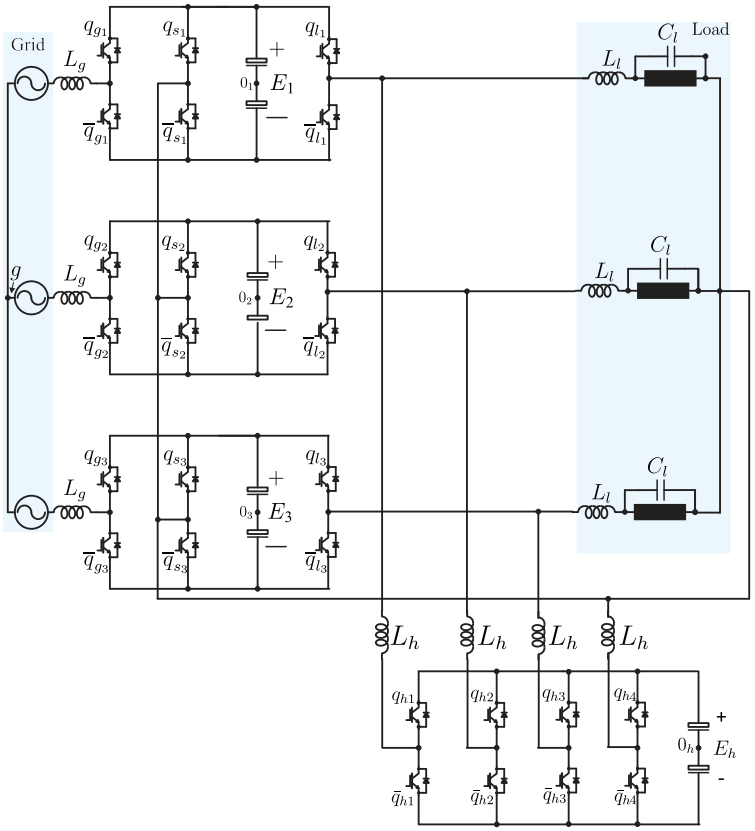
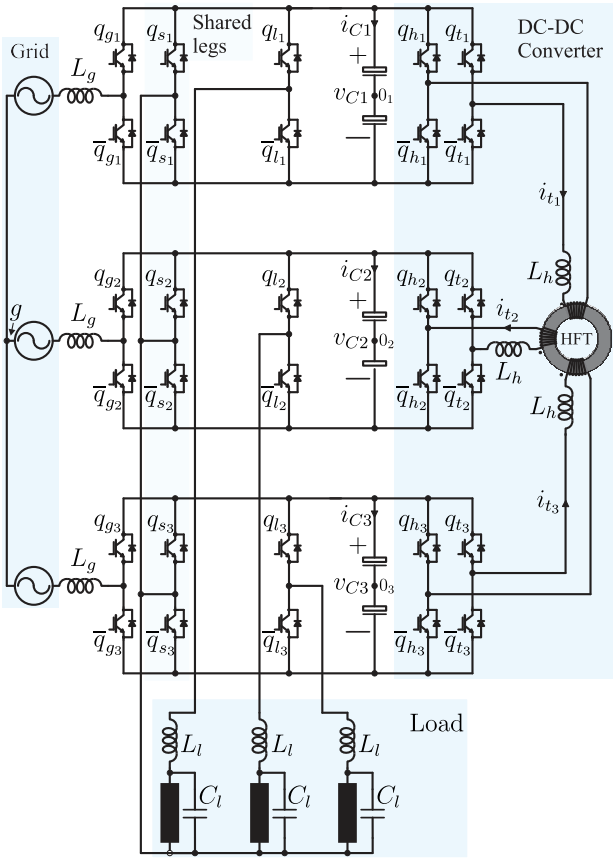


Figure 1.27 – 9LHF-UPQC configuration.



1.7 Scientific Production

As a result of this work, seven scientific papers were published or accepted for publication in international congresses of the IEEE (*Institute of Electrical and Electronic Engineers*), and three scientific articles were published in Qualis A1 journal:

- J. T. Cardoso, C. B. Jacobina, P. L. S. Rodrigues and A. M. N. Lima, "PUC Converter Based on AC-DC-AC Multilevel Topologies with a Shared Leg," 2021 IEEE Energy Conversion Congress and Exposition (ECCE), Vancouver, BC, Canada, 2021, pp. 2394-2401, doi: 10.1109/ECCE47101.2021.9595136.
- J. T. Cardoso, C. B. Jacobina, P. L. S. Rodrigues and A. M. N. Lima, "Single-Phase AC-DC-AC Multilevel Five-leg Converter Based on a High-Frequency Transformer," 2021 IEEE Energy Conversion Congress and Exposition (ECCE), Vancouver, BC, Canada, 2021, pp. 2501-2508, doi: 10.1109/ECCE47101.2021.9595904.
- J. T. Cardoso, C. B. Jacobina and A. S. Felinto, "Single-phase Transformerless Unified Power Quality Conditioner Based on Three-Leg Converter," 2022 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2022, pp. 1-8, doi: 10.1109/ECCE50734.2022.9948060.
- J. T. Cardoso, C. B. Jacobina, A. S. Felinto and M. B. R. Correa, "Five-Leg Single-Phase Transformerless Unified Power Quality Conditioner," 2022 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2022, pp. 1-8, doi: 10.1109/ECCE50734.2022.9947841.
- J. T. Cardoso, C. B. Jacobina, A. S. Felinto and M. B. R. Correa, "Three-Phase Four-Wire Unified Power Quality Conditioner Based on AC-DC-AC Nine-Leg Converter and Shunt Converter," 2022 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2022, pp. 1-8, doi: 10.1109/ECCE50734.2022.9947873.
- J. T. Cardoso, C. B. Jacobina, A. S. Felinto, A. A. Dos Santos and M. B. R. Correa, "Single-phase Transformerless Unified Power Quality Conditioner Based on Three-Leg and Standby Converters," 2023 IEEE Energy Conversion Congress and Exposition (ECCE), Nashville, TN, USA, 2023, pp. 2896-2903, doi: 10.1109/ECCE53617.2023.10362429.
- J. T. Cardoso, C. B. Jacobina, P. L. S. Rodrigues and A. M. N. Lima, "PUC Converter Based on AC-DC-AC Multilevel Topologies With a Shared Leg," in IEEE Transactions on Industry Applications, doi: 10.1109/TIA.2023.3292817.
- J. T. Cardoso, C. B. Jacobina, P. L. S. Rodrigues and A. M. N. Lima, "Single-Phase AC-DC-AC Multilevel Five-leg Converter Based on a High-Frequency Transformer," in IEEE Transactions on Industry Applications, doi: 10.1109/TIA.2023.3288513.

- J. T. Cardoso, A. S. Felinto, C. B. Jacobina and M. B. d. R. Corrêa, "Three-Phase Four-Wire Nine-Leg AC–DC–AC Converter Based on High-Frequency Link," in IEEE Transactions on Power Electronics, vol. 39, no. 1, pp. 885-897, Jan. 2024, doi: 10.1109/TPEL.2023.3327160.

- J. T. Cardoso, C. B. Jacobina, A. S. Felinto and M. B. d. R. Corrêa, "Three-Phase Four-Wire Nine-Leg Unified Power Quality Conditioner Based on AC-DC-AC Nine-Leg Converter and Shunt Converter," [Accepted for publication in: IEEE Transactions on Industry Applications].

- J. T. Cardoso, C. B. Jacobina, A. S. Felinto and M. B. d. R. Corrêa, "Five-Leg Single-Phase Transformerless Unified Power Quality Conditioner," [Accepted for publication in: IEEE Transactions on Industry Applications].

- J. T. Cardoso, C. B. Jacobina, A. S. Felinto, A. A. Santos Jr, and A. C. Oliveira, "A Transformerless Unified Power Quality Conditioner Based on Four-Leg Converter." [Accepted for publication in: 2024 IEEE Energy Conversion Congress and Exposition (ECCE)].

In addition to the articles mentioned, other scientific papers have been published at international congresses of the IEEE, but these are not part of the doctoral dissertation:

- J. T. Cardoso, A. Santana Felinto, C. B. Jacobina, M. Beltrão de Rossiter Corrêa and A. De Queiroz Tavares Borges Mesquita, "Three-Phase Unified Power Quality Conditioner in Open Delta With Shared Legs," 2023 IEEE Energy Conversion Congress and Exposition (ECCE), Nashville, TN, USA, 2023, pp. 1283-1290, doi: 10.1109/ECCE53617.2023.10362485.

- J. T. Cardoso, C. B. Jacobina, A. S. Felinto, A. A. Dos Santos and A. C. Oliveira, "Three-Phase Four-Wire Transformerless Unified Power Quality Conditioner Based on Single-phase and Three-Phase Cells," 2023 IEEE Energy Conversion Congress and Exposition (ECCE), Nashville, TN, USA, 2023, pp. 1310-1317, doi: 10.1109/ECCE53617

Chapter 2

Single-Phase AC-DC-AC Multilevel Five-leg Converter Based on a High-Frequency Transformer

2.1 Introduction

In an electrical system in which load voltage regulation, as well as harmonic and reactive current compensation are required, the UPQC system stands out since it integrates shunt and series modules. Conventional single-phase ac-dc-ac UPQC systems are composed of LFTs, inductive and capacitive filters, and two h-bridge inverters sharing the same dc link. Usually, given the increase in the total system cost and size, LFTs are not cost-effective (PENG et al., 2016). As solution, transformerless-based single-phase ac-dc-ac topologies were proposed, such as half-bridge and three-leg converters (ABDALAAL; HO, 2022; LU et al., 2016). In terms of cost-effectiveness, a three-leg converter is more intended since it reduces the number of power switches in comparison to a full-bridge converter and presents all switches with half of the reverse voltage compared to a half-bridge converter for the same load voltage amplitude.

Based on a three-leg converter, topologies with multilevel features were proposed for connecting a full-bridge configuration to the grid, load, or shared part of the converter. A configuration comprising one three-leg module with a series-connected full bridge to the shared part of the system is proposed in (MAIA; JACOBINA, 2014). Compared with the conventional three-leg, this topology demonstrated a better performance considering harmonic distortions and semiconductor power losses. On the other hand, by adding floating capacitors at dc links, the voltages must be regulated, which requires more complexity for the control system. Further, constraints are addressed in the modulation index, reactive

power compensation, and under grid voltage sags when it operates with asymmetrical dc-link voltages. Therefore, a symmetrical dc-link operation is the best scenario for this topology.

HFTs are another alternative to avoid the problems associated with LFTs, as in most cases they reduce the size, cost, and losses in voltage source inverters (LU et al., 2016). In this cotext, in this Chapter, a single-phase ac-dc-ac multilevel five-leg converter based on a HFT is investigated. The system consists of a three-leg module with a full-bridge module connected to the shared part of the system. In the proposed configuration, the dc link of the three-leg module is supplied by the full-bridge module through a single active bridge (SAB) converter. This feature improves the power quality and efficiency of the structure and simplifies the design of the control strategy compared to the conventional solution that uses floating capacitors. The proposed system is composed of a shunt unit and a series unit. The first one is responsible for compensating reactive power and harmonic currents, while the second provides load voltage compensation against voltage sags and harmonics in the grid voltage. In addition, the proposed converter operates with low dc-link voltages in applications with the same input and output frequency, such as unified power quality conditioner (UPQC). The model of the system, a space-vector pulse-width modulation (PWM) and the overall control scheme are addressed. Simulations and experimental results are presented to confirm the feasibility of the proposed converter and the correctness of the design methodology.

2.2 System Model

Fig. 2.1 shows the proposed five-leg ac-dc-ac converter based on high-frequency link (HFL). Such a configuration consists of a three-leg module with a full-bridge module connected to the shared leg, inductor and capacitor filters (L_g, L_l, C_l), and two dc links (C_a,C_b). The full-bridge converter (h-bridge) has a dc-link voltage E_b (B) that feeds the three-leg dc-link voltage E_a (A) through a single active bridge (SAB) converter. The SAB converter consists of an active and passive bridge connected via an HFT. The proposed configuration includes switches $q_j - \bar{q}_j$, with $j \in \{g, l, s, sa, sb, b\}$. The switch pairs $q_j - \bar{q}_j$ are complementary, and the switching state is given by $q_j = 0$ when the switch is open and $q_j = 1$ when it is closed. In addition, the proposed system is fed by a single-phase grid whose voltage and current are denoted by e_g and i_g, respectively, and supplies a load whose voltage and current are denoted by e_l and i_l. The series unit is formed by legs l, s, sa, and sb, while the shunt unit is formed by legs g, s, sa, and sb. Notice that, legs s, sa, and sb are common to both the series and shunt units. The LC filter (L_l,C_l) on the series side is used as a low-pass filter to eliminate the high-frequency components of the load voltage, while the L_g filter is used to connect the grid voltage to the shunt unit and smooth the grid current ripple.

Figure 2.1 – Proposed 5L-HFL Converter.

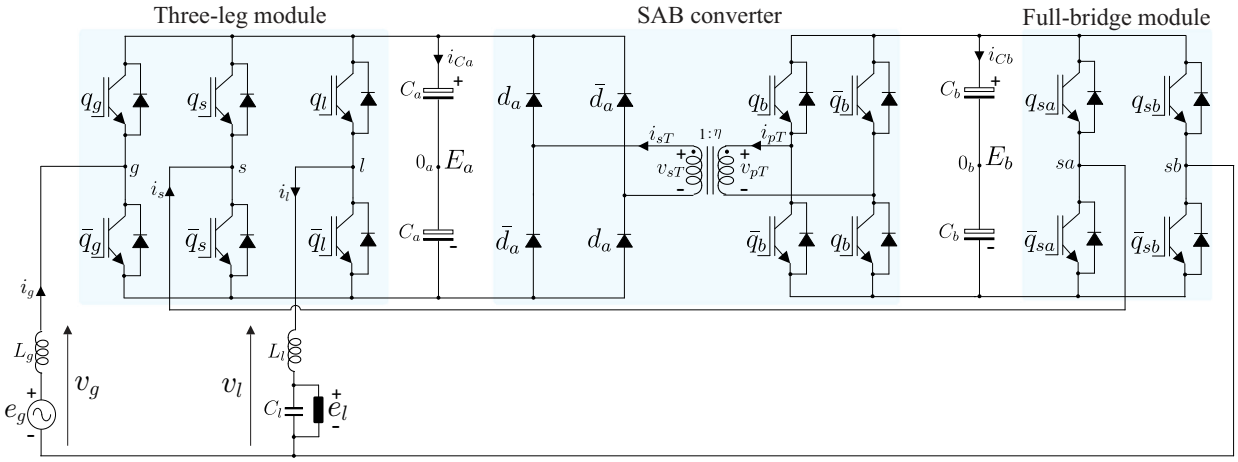
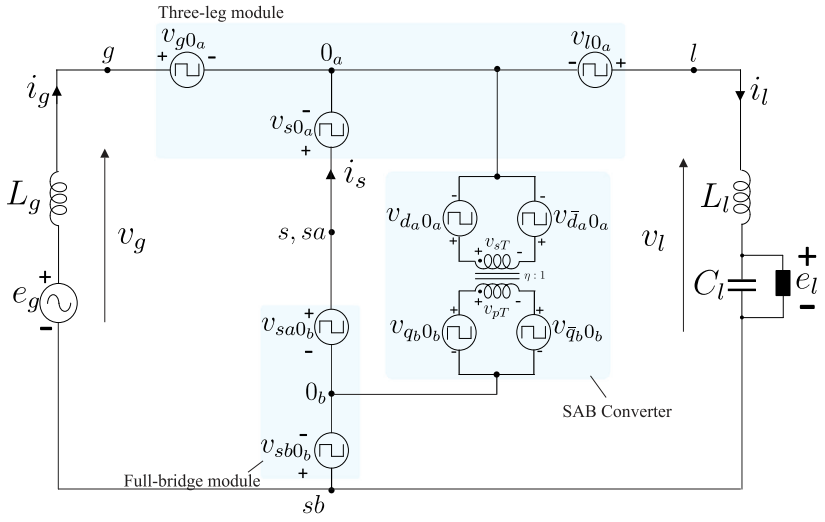


Fig. 2.2 presents the simplified equivalent circuit of the proposed converter based on the pole voltages. The pole voltage of each leg is represented by a voltage source and is calculated considering the voltage between the midpoints of a leg and its dc-link. In this way, the pole voltages are limited to half of their respective dc-link voltage (e.g., $|v_{g0a}| \leq E_a/2$). The equations describing the system model are obtained from Kirchhoff's law and are given by

Figure 2.2 – Simplified circuit.



$$e_g = v_g + Z_g i_g, \tag{2.1}$$

$$e_l = v_l - Z_l i_l, \tag{2.2}$$

$$i_s = i_l - i_g, \tag{2.3}$$

where v_g and v_l are the shunt and series converter voltages generated by the rectifier and inverter side, respectively; i_s is the shunt compensation current, and $Z_g = R_g + sL_g$ and $Z_l = R_l + sL_l$ represent the impedance of inductors L_g and L_l, respectively. Applying Kirchhoff's voltage law to the circuit, the voltages v_g and v_l can be calculated as a function of pole voltages, respectively, as

$$v_g = v_{g0_a} - v_{s0_a} + v_{sa0_b} - v_{sb0_b}, \tag{2.4}$$

$$v_l = v_{l0_a} - v_{s0_a} + v_{sa0_b} - v_{sb0_b}. \tag{2.5}$$

In this case, the pole voltages can be calculated generically defining the dc-link voltages as a function of the transformer turn ratio, represented as η. Since $\eta = E_b/E_a$ and $E_a + E_b = E$, the pole voltages of the three-leg and two-leg modules are calculated, respectively, by

$$v_{x0_a} = (2q_x - 1)\,\frac{E}{2 + 2\eta}, \text{ with } x \in \{g, l, s\}, \tag{2.6}$$

$$v_{y0_b} = (2q_y - 1)\frac{\eta E}{2 + 2\eta}, \text{ with } y \in \{sa, sb\}. \tag{2.7}$$

2.2.1 Dc-link Voltage Specifications and Synchronization

Henceforward the symbol * denotes a reference variable. Since the dc-link voltages E_a and E_b can be defined as a function of the v_g and v_l, the following conditions must be satisfied to generate correctly the voltages

$$|v_g^*| \leq E^*, \tag{2.8}$$

$$|v_l^*| \leq E^*, \tag{2.9}$$

$$|v_g^* - v_l^*| \leq \frac{E^*}{1 + \eta}. \tag{2.10}$$

From trigonometric analysis and considering equations (2.8)-(2.10), it is possible to obtain

$$\theta_{lg} = \arccos\left(\frac{V_g^{*2} + V_l^{*2} - \left(\frac{E^*}{1+\eta}\right)^2}{2V_g^* V_l^*}\right), \tag{2.11}$$

where θ_{lg} is the angle between v_g and v_l that must be respected, and V_g^* and V_l^* are the shunt and series reference voltage amplitude, respectively. Table 2.1 shows the voltages, number of voltage levels, and the range in which angle θ_{lg} must be considered, according to the transformer turn ratio, for the proposed topology. As observed, the proposed topology generates input and output voltages, v_g and v_l, with the same number of levels for the three employed turn ratio specifications. When $E_b = E_a$ the proposed one produces only five levels. By using asymmetrical dc-link voltages, $E_b = 2E_a$ and $E_b = 3E_a$, the converter produces, respectively, up to seven and nine levels with minimum dc-link voltages values necessary to synthesize v_g and v_l.

Table 2.1 – Transformer turn ratios, levels of v_g and v_l, and range of θ_{lg}.

$\eta = E_b^*/E_a^*$	E_a^*	E_b^*	Nº of levels of v_g and v_l	$\lvert\theta_{lg}\rvert$
$\eta = 1$	0.50	0.50	5	$\lvert\theta_{lg}\rvert \leq 28.9°$
$\eta = 2$	0.33	0.66	7	$\lvert\theta_{lg}\rvert \leq 19.2°$
$\eta = 3$	0.25	0.75	9	$\lvert\theta_{lg}\rvert \leq 14.3°$

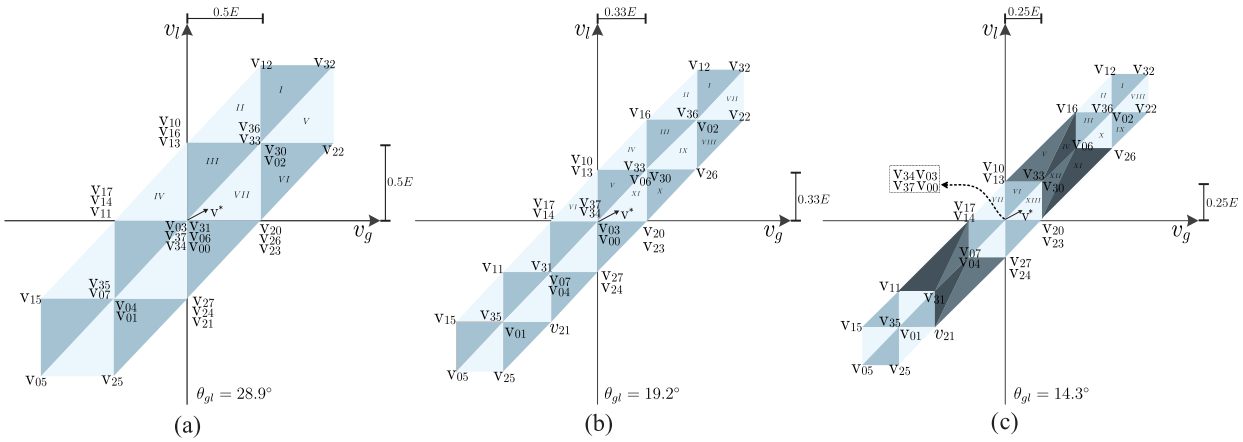
2.3 PWM Strategy

2.3.1 Ac-dc-ac converter

A space-vector PWM strategy (SV-PWM) is developed for $\eta = 1$, 2, and 3, in order to control the ac-dc-ac 5L-HFL. Fig. 2.3 presents the space-vector planes generated by the converter for the three cases. Each triangle represents a sector and each vertex is a voltage vector. A voltage vector can be generated by a given switching combination and is denoted by

$$\mathbf{v} = v_g + jv_l. \tag{2.12}$$

Figure 2.3 – Space-vector plans generated by the proposed converter. (a) $E_b = E_a$ ($\eta = 1$). (b) $E_b = 2E_a$ ($\eta = 2$). (c) $E_b = 3E_a$ ($\eta = 3$).



The voltages v_g and v_l represent the real axis (Re) and imaginary axis (Im), respectively. The vectors in the plane are represented as $\mathbf{v}_{k_a k_b}$, where k_a and k_b are the binary sequences $\{q_g, q_l\}$ and $\{q_s, q_{sa}, q_{sb}\}$, respectively, converted to decimal numbers. For example, the voltage vector $\mathbf{v}_{32}$ corresponds to $\{q_g,\ q_l,\ q_s,\ q_{sa},\ q_{sb}\} = \{1,\ 1,\ 0,\ 1,\ 0\}$.

Consider that $\mathbf{v}^* = v_g^* + \mathrm{j}v_l^*$ represents the reference voltage vector that must be generated by the converter during the sampling period $T_s = 1/f_s$. The reference voltage located within a sector is synthesized by the three nearest voltage vectors, which are located at the vertices of the triangle. These vectors are defined as $\mathbf{v}_x$, $\mathbf{v}_y$, and $\mathbf{v}_z$. Taking into account a constant reference voltage $\mathbf{v}^*$ during a sampling period T_s, it can be determined

$$\mathbf{v}^* = \tau_x \mathbf{v}_x + \tau_y \mathbf{v}_y + \tau_z \mathbf{v}_z, \tag{2.13}$$

where τ_x, τ_y, and τ_z represents the duty cycles of the three nearest vectors $\mathbf{v}_x$, $\mathbf{v}_y$, and $\mathbf{v}_z$, respectively. The duty cycle of each vector can be calculated by

$$\begin{bmatrix} \tau_x \\ \tau_y \\ \tau_z \end{bmatrix} = \begin{bmatrix} \mathrm{Re}(\mathbf{v}_x) & \mathrm{Re}(\mathbf{v}_y) & \mathrm{Re}(\mathbf{v}_z) \\ \mathrm{Im}(\mathbf{v}_x) & \mathrm{Im}(\mathbf{v}_y) & \mathrm{Im}(\mathbf{v}_z) \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} v_g^* \\ v_l^* \\ 1 \end{bmatrix}. \tag{2.14}$$

Table 2.2 defines the SV-PWM sequences in order to minimize the switching losses for $\eta = 1$, 2, and 3. Due to the space-vector plane symmetry, it was considered only the quadrants in which $v_l^* \geq 0$.

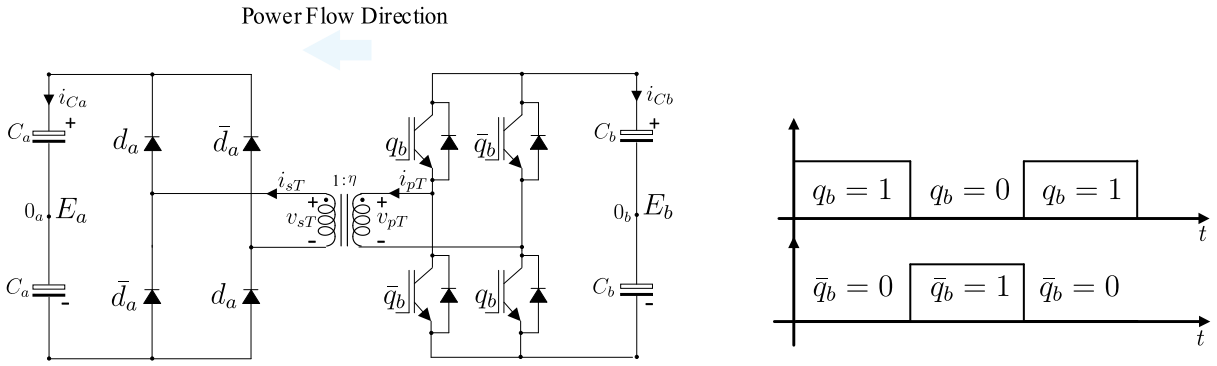
Table 2.2 – Sequences of vectors applied for $\eta = 1$, 2, and 3 to minimize the switching losses.

Sector	Sequences		
	$\eta = 1$	$\eta = 2$	$\eta = 3$
I	$\mathbf{v}_{30}$ - $\mathbf{v}_{32}$ - $\mathbf{v}_{12}$	$\mathbf{v}_{32}$ - $\mathbf{v}_{12}$ - $\mathbf{v}_{02}$	$\mathbf{v}_{32}$ - $\mathbf{v}_{12}$ - $\mathbf{v}_{02}$
II	$\mathbf{v}_{13}$ - $\mathbf{v}_{12}$ - $\mathbf{v}_{30}$	$\mathbf{v}_{16}$ - $\mathbf{v}_{12}$ - $\mathbf{v}_{02}$	$\mathbf{v}_{16}$ - $\mathbf{v}_{12}$ - $\mathbf{v}_{02}$
III	$\mathbf{v}_{33}$ - $\mathbf{v}_{13}$ - $\mathbf{v}_{06}$	$\mathbf{v}_{16}$ - $\mathbf{v}_{06}$ - $\mathbf{v}_{02}$	$\mathbf{v}_{16}$ - $\mathbf{v}_{06}$ - $\mathbf{v}_{02}$
IV	$\mathbf{v}_{13}$ - $\mathbf{v}_{17}$ - $\mathbf{v}_{06}$	$\mathbf{v}_{33}$ - $\mathbf{v}_{13}$ - $\mathbf{v}_{16}$	$\mathbf{v}_{30}$ - $\mathbf{v}_{16}$ - $\mathbf{v}_{06}$
V	$\mathbf{v}_{32}$ - $\mathbf{v}_{22}$ - $\mathbf{v}_{02}$	$\mathbf{v}_{00}$ - $\mathbf{v}_{10}$ - $\mathbf{v}_{30}$	$\mathbf{v}_{16}$ - $\mathbf{v}_{10}$ - $\mathbf{v}_{30}$
VI	$\mathbf{v}_{26}$ - $\mathbf{v}_{22}$ - $\mathbf{v}_{02}$	$\mathbf{v}_{00}$ - $\mathbf{v}_{10}$ - $\mathbf{v}_{14}$	$\mathbf{v}_{30}$ - $\mathbf{v}_{10}$ - $\mathbf{v}_{00}$
VII	$\mathbf{v}_{26}$ - $\mathbf{v}_{06}$ - $\mathbf{v}_{02}$	$\mathbf{v}_{32}$ - $\mathbf{v}_{22}$ - $\mathbf{v}_{02}$	$\mathbf{v}_{14}$ - $\mathbf{v}_{10}$ - $\mathbf{v}_{00}$
VIII		$\mathbf{v}_{26}$ - $\mathbf{v}_{22}$ - $\mathbf{v}_{02}$	$\mathbf{v}_{32}$ - $\mathbf{v}_{22}$ - $\mathbf{v}_{02}$
IX		$\mathbf{v}_{02}$ - $\mathbf{v}_{06}$ - $\mathbf{v}_{26}$	$\mathbf{v}_{26}$ - $\mathbf{v}_{22}$ - $\mathbf{v}_{02}$
X		$\mathbf{v}_{26}$ - $\mathbf{v}_{20}$ - $\mathbf{v}_{30}$	$\mathbf{v}_{26}$ - $\mathbf{v}_{06}$ - $\mathbf{v}_{02}$
XI		$\mathbf{v}_{00}$ - $\mathbf{v}_{20}$ - $\mathbf{v}_{30}$	$\mathbf{v}_{06}$ - $\mathbf{v}_{26}$ - $\mathbf{v}_{23}$
XII			$\mathbf{v}_{30}$ - $\mathbf{v}_{20}$ - $\mathbf{v}_{06}$
XIII			$\mathbf{v}_{30}$ - $\mathbf{v}_{20}$ - $\mathbf{v}_{00}$

2.3.2 Single active bridge dc-dc converter

The active bridge of the SAB converter is controlled by pulse-width modulation with a constant duty cycle, generating a square-wave voltage on v_{pT}. The switching signals of $\{q_b, \bar{q}_b\}$ and the correct power flow direction are described in Fig. 2.4.

Figure 2.4 – Power flow direction in the HFL and switching states.



2.4 Power Flow Analysis

Neglecting the converter power losses, the processing power over 5L-HFL converter is given by

$$P_{in} = P_{Ca} + P_{Cb} + P_{out}, \tag{2.15}$$

where P_{in} and P_{out} are the power delivered from the input to output of the converter, respectively. P_{Ca} and P_{Cb} are the power in the dc links of the three-leg and two-leg modules, respectively. Considering $P_{in} = v_g i_g$ and $P_{out} = v_l i_l$, it can be determined

$$P_{in} = (v_{g0_a} - v_{s0_a})i_g + (v_{sa0_b} - v_{sb0_b})i_g, \tag{2.16}$$

$$P_{out} = (v_{l0_a} - v_{s0_a})i_l + (v_{sa0_b} - v_{sb0_b})i_l. \tag{2.17}$$

Then, combining (2.15), (2.16), and (2.17), P_{Ca} and P_{Cb} can be written as follows

$$P_{Ca} = v_{g0_a} i_g - v_{l0_a} i_l + v_{s0_a} i_s, \tag{2.18}$$

$$P_{Cb} = (v_{sb0_b} - v_{sa0_b})i_s. \tag{2.19}$$

Since the proposed system is composed by a SAB converter, the power flow direction goes from the dc-link B to the dc-link A. According to (2.18) and (2.19), the instantaneous

power in each dc-link depends on the switching states of the converter and the grid and load currents. In this way, it is possible to define the operating regions from the space-vector plans where the dc-link A operates delivering power (discharging the capacitors C_a) and the dc-link B receiving power (charging the capacitors C_b), which eliminates the need for voltage and current sensors to control the dc-link voltage E_a.

Table 2.3 – Parameters Considered For Tests.

Parameter		Value
Grid voltage amplitude	E_g	311 V
Load reference voltage amplitude	E_l^*	311 V
Load power	P_l	2000 W
Modulation index	m	0.975
Sampling frequency	f_s	10 kHz
Grid power factor	$\cos(\gamma_g)$	1.0
Load power factor	$\cos(\gamma_l)$	0.8^*
Grid inductance	L_g	3.5 mH

The system voltages and currents in steady state are $\mathbf{E}_g = E_g\angle\delta_g$, $\mathbf{V}_g = V_g\angle\theta_g$, $\mathbf{I}_g = I_g\angle\delta_g$, $\mathbf{V}_l = V_l\angle\theta_l$, and $\mathbf{I}_l = I_l\angle(\theta_l + \gamma_l)$. V_g and V_l are the shunt and series converter voltage amplitudes, respectively, while I_g and I_l are the grid and load current amplitudes, respectively. θ_g and θ_l is the phase angle of v_g and v_l, respectively, and γ_g and γ_l are the grid and load power factor angles, respectively. To analyze the instantaneous power, steady-state simulations were performed considering a variation in the load power factor from $\cos(\gamma_l) = 0.5$ to 1 and the range of the angle θ_{lg} for all cases shown in Table 2.1. Furthermore, the parameters presented in Table 2.3 were employed and the sequence of vectors in each sector of the space-vector planes was chosen in order to minimize switching losses (see Table 2.2). Fig. 2.5 presents the instantaneous powers P_{Ca} and P_{Cb} of the dc links A and B, respectively. The first and second columns show the operating regions in rated conditions ($E_g = 220$ V) and the third and fourth columns present the operations regions under 20% of voltage sag ($E_g = 176$ V). As can be seen, for all cases, the correct flow direction can be guaranteed when the load voltage phase angle θ_l ($= \theta_{lg} + \theta_g$) is calculated for P_{Ca} negative and P_{Cb} positive. Under rated conditions, the proposed system operates correctly for negative values of θ_{lg}. In case of voltage sags scenarios, the operating range increases, mainly for $\eta = 2$ and $\eta = 3$, where the proposed converter can handle this disturbance for any value of θ_{lg}.

Although not considered in this work, the regulation of the dc-link voltage E_a for any value of θ_{lg} can be achieved by considering the redundant voltage vectors and their capacitor-current contributions. In each sector of the space-vector planes presented in Fig. 2.3, may exist some possibilities of choosing the three closest vectors to be applied to produce the reference voltage vector $\mathbf{v}^*$. These redundancies can be selected in order to

regulate the dc-link voltages, since some redundant vectors may have different current contributions. The current through the dc-link capacitor C_a is given by

$$i_{Ca} = (q_g - q_l)i_g + (q_s - q_l)i_s \tag{2.20}$$

As expected, the current through the capacitor C_a depends on the switching states of the three-leg module. To ensure the proper power flow direction, the voltage vector sequence chosen must also consider, at least, shunt compensation current polarity. To exemplify, consider the space-vector plane in which $E_a = E_b$. In the sector I, the vector sequence that ensures the discharge when $i_s \geq 0$ are $\mathbf{v}_{32} \Rightarrow \mathbf{v}_{30} \Rightarrow \mathbf{v}_{12} \Rightarrow \mathbf{v}_{30} \Rightarrow \mathbf{v}_{32}$. Notice that the only vector that can be changed for sector I is $\mathbf{v}_{30}$. If $i_s < 0$ the vectors that can replace $\mathbf{v}_{30}$ are $\mathbf{v}_{36}$ and $\mathbf{v}_{32}$. Table 2.4 summarize the capacitor-current contributions considering $i_s \geq 0$. This method for balancing the dc links is based on at least two switching sequences, one for $i_s \geq 0$ and one $i_s < 0$, which increases the switching losses. Furthermore, an additional current sensor need to be used for proper implementation.

Table 2.4 – Capacitor-current contribution in E_a.

q_g-q_l-q_s	i_{Ca}	Contribution in E_a (for $i_s > 0$)
0-0-0	0	-
0-0-1	i_s	charge
0-1-0	$-i_l$	discharge
0-1-1	$-i_g$	charge
1-0-0	i_g	discharge
1-0-1	i_l	charge
1-1-0	$-i_s$	discharge
1-1-1	0	-

2.5 Control System

In this section, the control strategy for the proposed converter is discussed, including the shunt, series, and dc-link voltages control. Fig. 2.6 shows the control diagram for the studied configuration. To adjust the average value of the dc-link voltage E_b, a conventional proportional-integral controller is used. This block yields the amplitude of the reference grid current, represented as I_g^*. To ensure the grid power factor compensation, the instantaneous reference current i_g^*, is synchronized with the grid voltage e_g using a single-phase Phase-Locked Loop (PLL) block. The shunt control is performed by a resonant controller whose model is described in (JACOBINA et al., 2001). This block is responsible for generating the shunt reference voltage v_g^*. The load reference voltage e_l^* is determined considering the limits of the angle θ_{lg} (see Table 2.1) and the series reference voltage v_l^* is also defined by a resonant controller with constant magnitude and frequency.

Figure 2.5 – Power distribution P_{Ca} and P_{Cb} of dc-links A and B for all transformer ratio cases and considering the operation under rated conditions and under 20% of voltage sag.

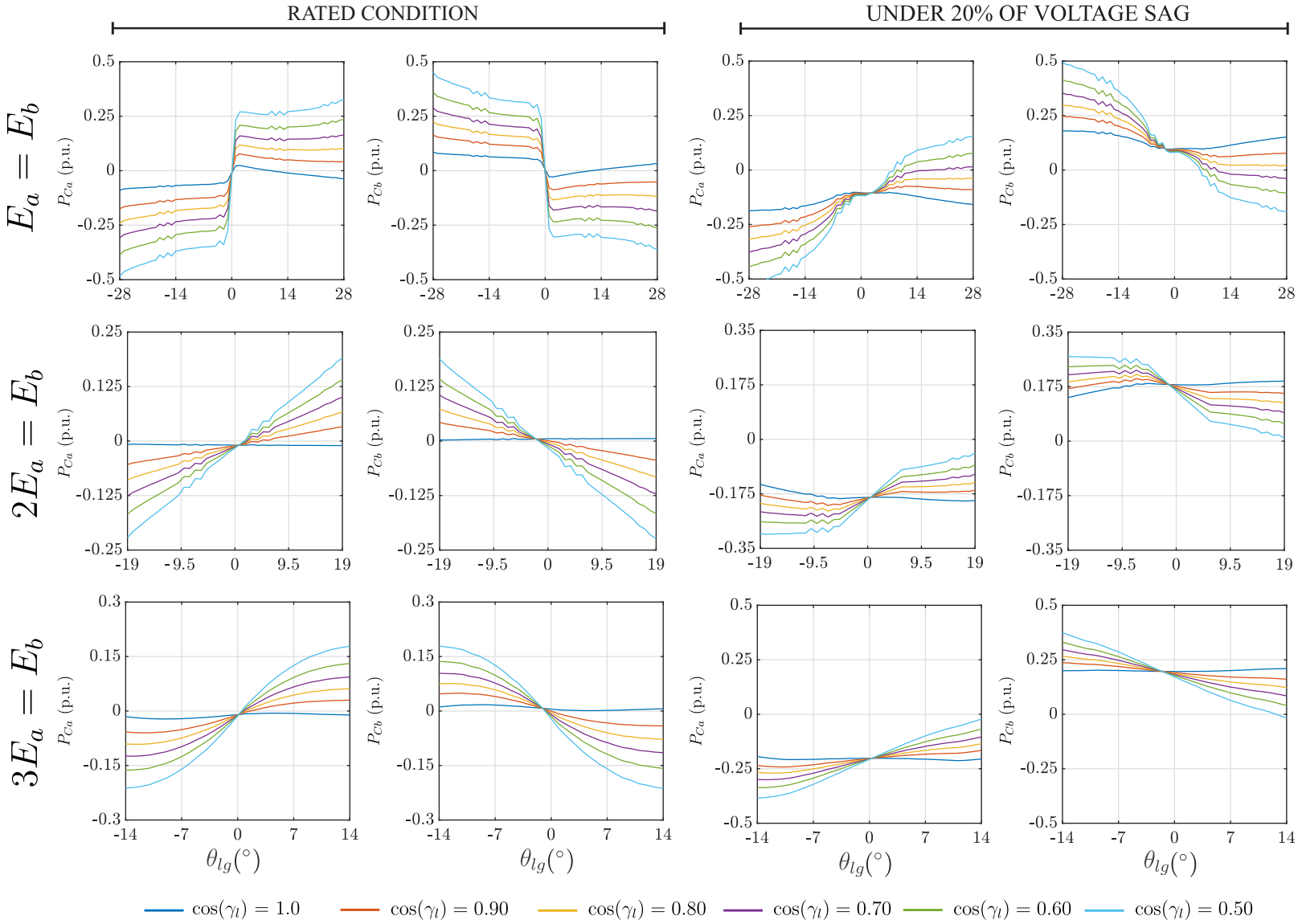
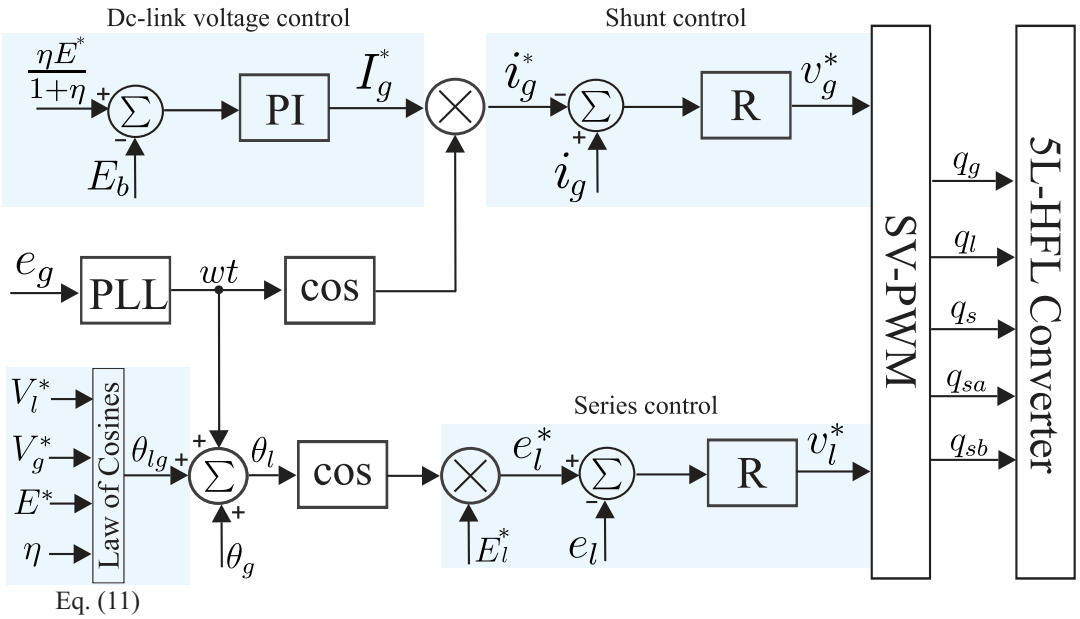


Figure 2.6 – Control block diagram.



2.6 Results

Simulation and experimental results in closed-loop control are shown to demonstrate the feasibility of the proposed converter. Power devices from Semikron, with IGBT SKM50GB123D, fast diode-modules SKKD60F17, and drivers SKHI23 were used in the setup (see Fig. 2.7). Furthermore, the converter was controlled using a digital signal processor (DSP) TMS320F28335 from Texas Instruments. The parameters used in both simulation and experimental tests are presented in Table 2.5. Also, Table 2.6 presents the specifications of the high-frequency core. The transformer used in the experimental tests is composed of six windings which allow connecting in series to form the primary or secondary windings of the transformer.

2.6.1 Simulation Results

Simulation results have been performed in order to demonstrate the capability of the proposed converter to compensate harmonic and reactive current, as well as, harmonic and sags disturbances in the grid voltage, ensuring shunt and series compensation. The results were obtained for $\eta = 2$ and 3.

Firstly, the capability of series and shunt compensation simultaneously was verified considering a grid voltage composed of 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic, as well as a nonlinear load with about 70% of harmonic

Table 2.5 – Parameters used in simulations and experimental tests.

Parameters		Value
Grid voltage amplitude	E_g	155.6 V
Series reference voltage amplitude	V_l	155.6 V
Transformer turn ratio	η	3
Sampling frequency	f_s	10 kHz
HFL sampling frequency	f_t	10 kHz
Dc-link capacitors	C_a, C_b	2.2 mF
Grid inductance	L_g	3.5 mH
RL load		
Load resistance	R_f	45 Ω
Load inductance	L_f	14 mH
Load filter inductance	L_l	2 mH
Load filter capacitance	C_l	18 μF
Nonlinear load I		
Total dc-link reference voltage	E^*	160 V
Apparent power	S_l	1.9 kVA
Load current	THD_{il}	70%
Nonlinear load II		
Total dc-link reference voltage	E^*	160 V
Apparent power	S_l	0.863 kVA
Load current	THD_{il}	47%

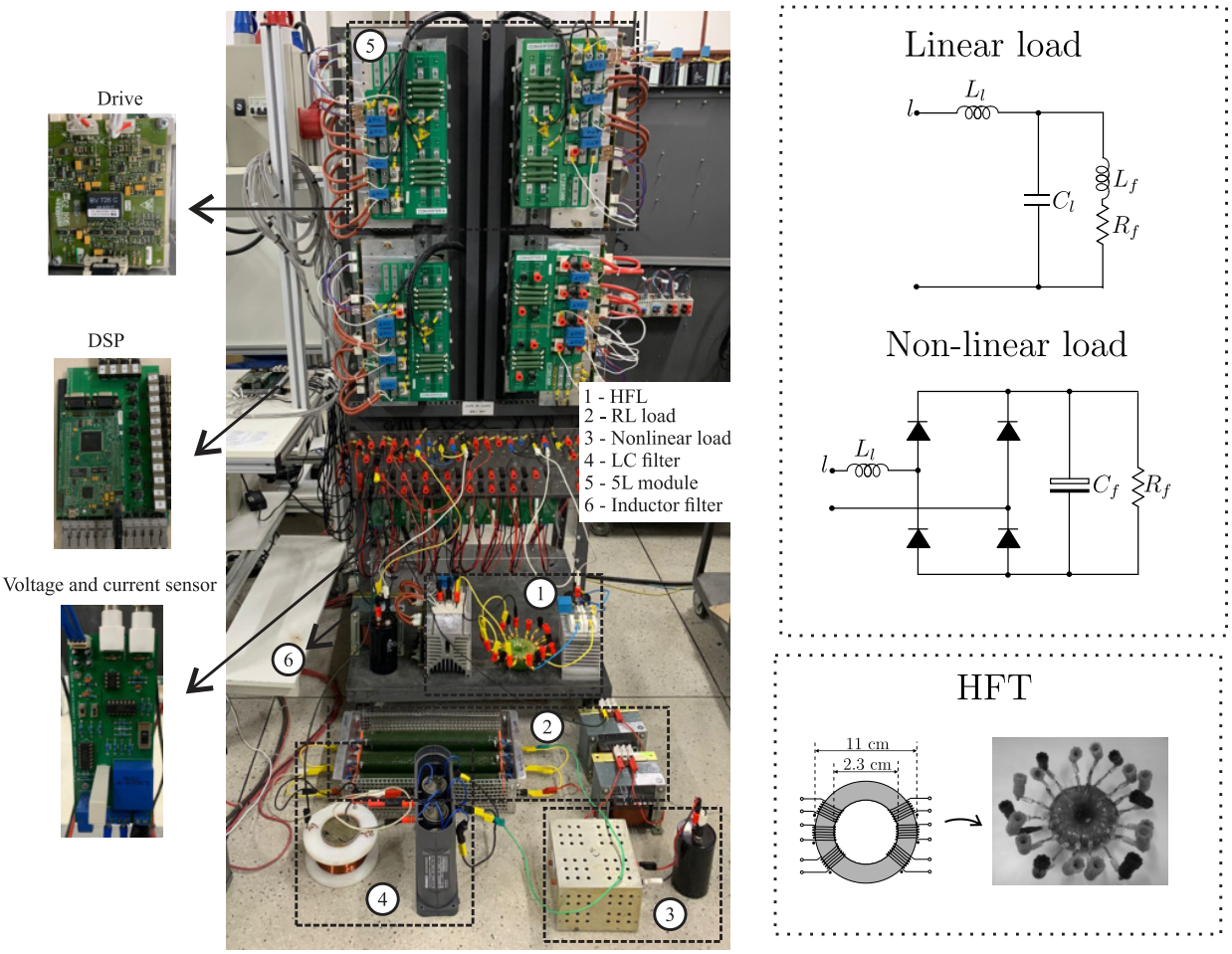
Table 2.6 – Parameters of The HFT used in simulations and experimental tests.

Parameters	Value
Core material	Nanocrystalline
Rated power	4 kVA
Operating frequency	10 kHz
Turn ratio	1 : 1 : 1 : 3
Number of windings	6
Leakage inductance	1 μH
Magnetizing inductance	137 mH
Series resistance	50 mΩ

distortion and 1.9 kVA (Nonlinear load I). Theses results were performed in steady state and are depicted in Figs. 2.8 and 2.9 for $\eta = 2$ and $\eta = 3$, respectively. Notice that in both scenarios, the grid current presents a sinusoidal waveform and is in phase with the grid voltage, ensuring the grid power factor close to the unity. Additionally, the average voltage of the series converter voltage is compensated.

Then, transient tests were done to verify the feasibility of the proposed control system (RL load and Nonlinear load II). Initially, the capability of the proposed converter

Figure 2.7 – Experimental setup for the 5L-HFL converter.



to compensate grid voltage sags has been demonstrated in Figs. 2.10 ($\eta = 2$) and 2.12 ($\eta = 3$) by applying a voltage sag of 20% at the moment t = 2 s to t = 3 s. In these tests, it was considered the linear load presented in Fig. 2.7. As can be seen, the load voltage e_l and dc-link voltages remain regulated in their reference value after and before the disturbance.

For the shunt test, Figs. 2.11 and 2.13 shows the system performance using a typical nonlinear load [see Fig. 2.7]. To validate the control system, a load transient, which increased the load power in about 45%, was applied. It can be noticed that, before and after the transient, the dc-link voltages remains controlled in their reference values, as well as the grid current presents low harmonic distortion and are in phase with the grid voltage, ensuring grid high grid power factor.

Figure 2.8 – Simulation results of the proposed converter in steady state for $\eta = 2$. (a) Grid voltage with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic. (b) Load current and shun compensation current. (c) Voltage (v_{pT}) and current (i_{pT}) in the primary side of the transformer. (d) Voltage (v_{sT}) and current (i_{sT}) in the secondary side of the transformer. (e) Dc-link voltages E_a. (f) Dc-link voltages E_b. (g) Shunt converter voltage. (h) Series converter voltage.

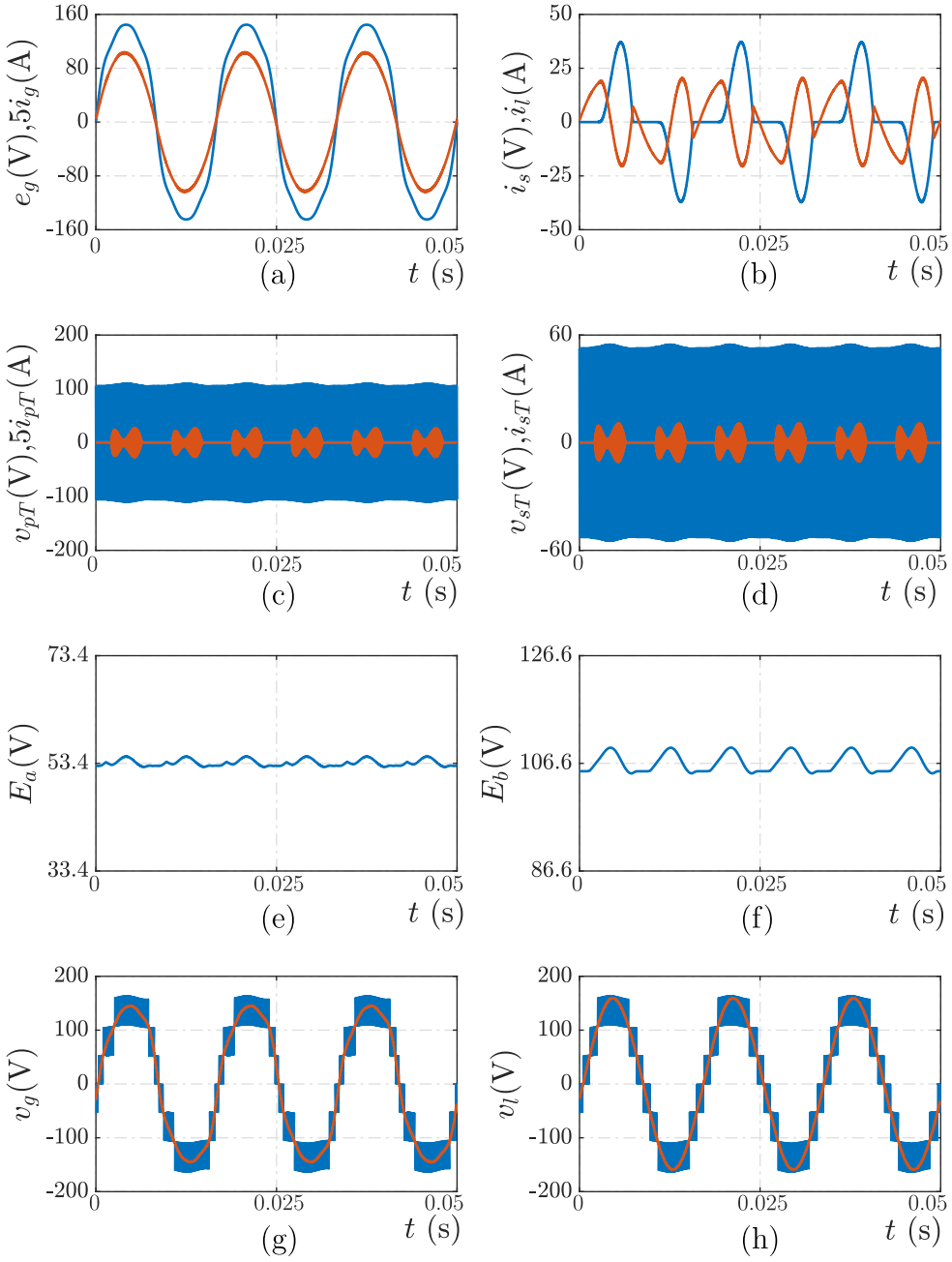


Figure 2.9 – Simulation results of the proposed converter in steady state for $\eta = 2$. (a) Grid voltage with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic. (b) Load current and shun compensation current. (c) Voltage (v_{pT}) and current (i_{pT}) in the primary side of the transformer. (d) Voltage (v_{sT}) and current (i_{sT}) in the secondary side of the transformer. (e) Dc-link voltages E_a. (f) Dc-link voltages E_b. (g) Shunt converter voltage. (h) Series converter voltage.

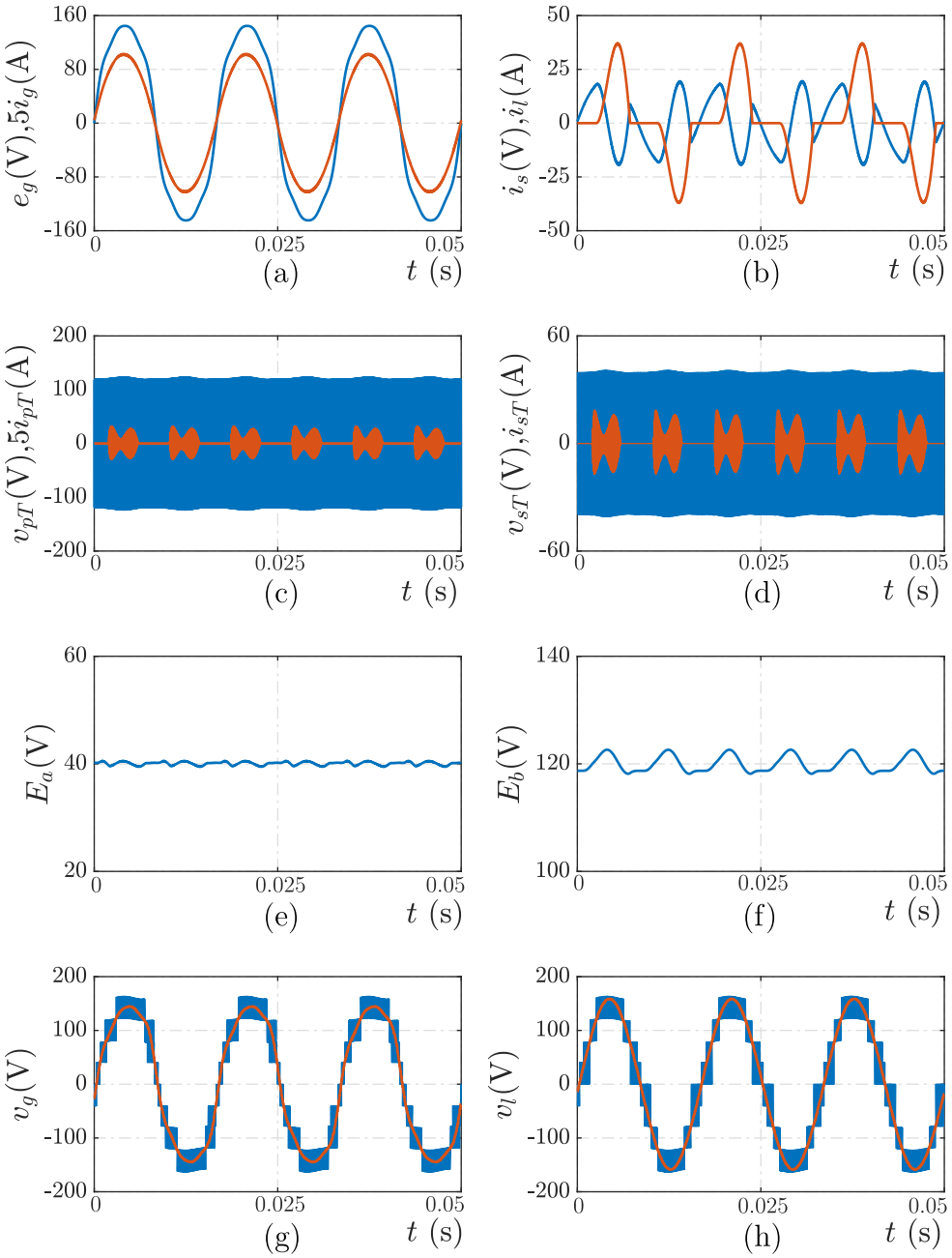


Figure 2.10 – Simulation results of the proposed converter under a voltage sag of 20% for $\eta = 2$.

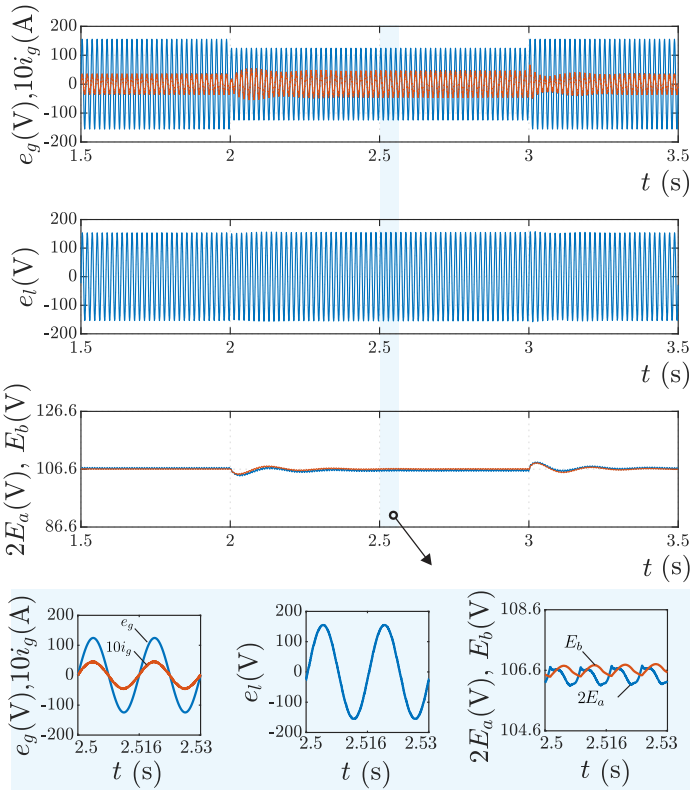


Figure 2.11 – Simulation results of the proposed converter during a trasient caused by a load power increase of 45% for $\eta = 2$.

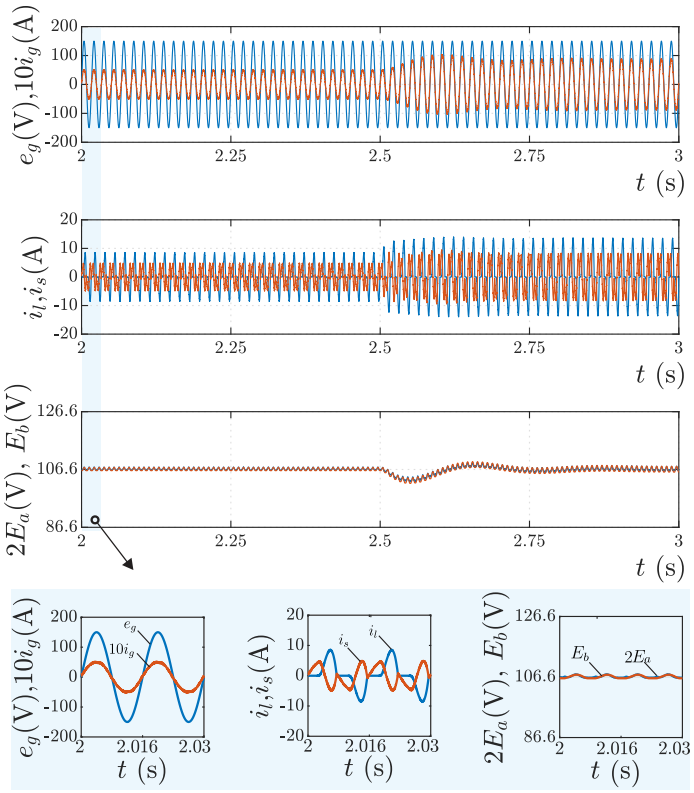


Figure 2.12 – Simulation results of the proposed converter under a voltage sag of 20% for $\eta = 3$.

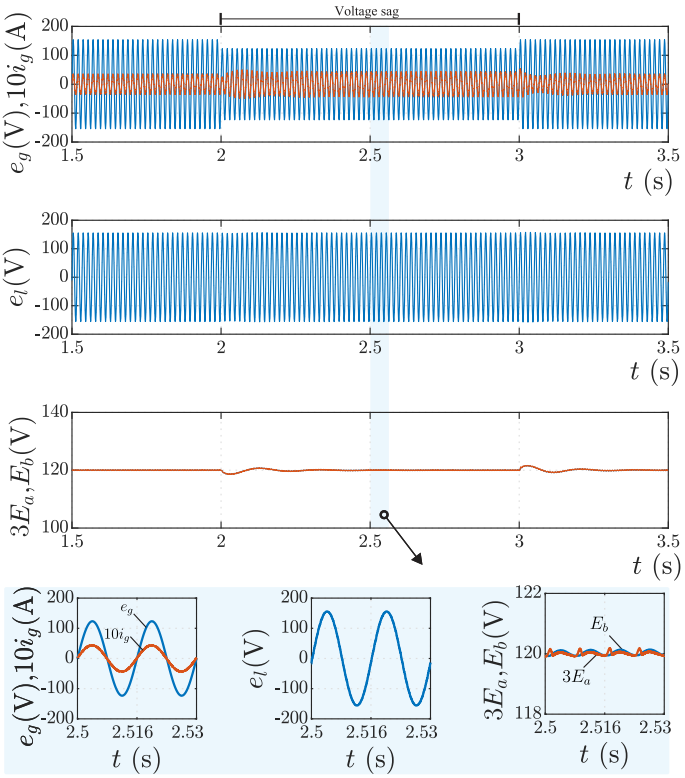
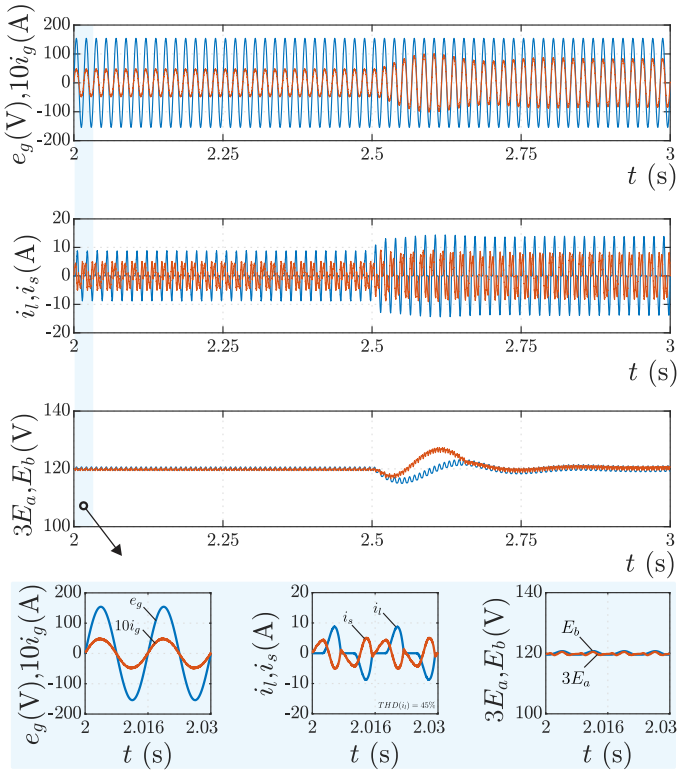


Figure 2.13 – Simulation results of the proposed converter during a trasient caused by a load power increase of 45% for $\eta = 3$.



2.6.2 Experimental Results

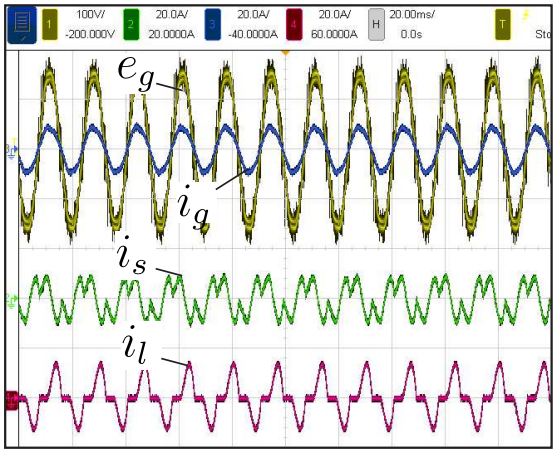
The experimental tests was performed also for $\eta = 2$ and $\eta = 3$. Initially, Fig. 2.14 shows experimental results in a steady state for $\eta = 2$. From top to bottom, Fig. 2.14(a) presents the grid voltage (e_g) and current (i_g) in phase, as well as, the shunt compensation current (i_s), and the load current (i_l). From top to bottom, Fig. 2.14(b) presents the voltage generated by the shunt (v_g) and series (v_l) sides with seven levels, as expected. Lastly, Fig. 2.14(c) depicts the voltages (v_{pT}, v_{sT}) and currents (i_{pT}, i_{sT}) at the primary and secondary windings of the HFT. The amplitude of the 10 kHz square-wave voltage v_{pT} and v_{sT} is determined by the transformer turn ratio selected. The currents at the primary and secondary windings also oscillate in 10 kHz and their amplitude alters according to the instantaneous power in the dc links P_{Ca} and P_{Cb}.

Fig. 2.15 validates the operation of the proposed configuration under 20% of grid voltage sag for $\eta = 2$. In this case, all the tests were performed using the aforementioned linear load. Notice that, the load voltage e_l keeps in its rated value during the sag event. Furthermore, the dc-link also remains controlled in their reference voltage value.

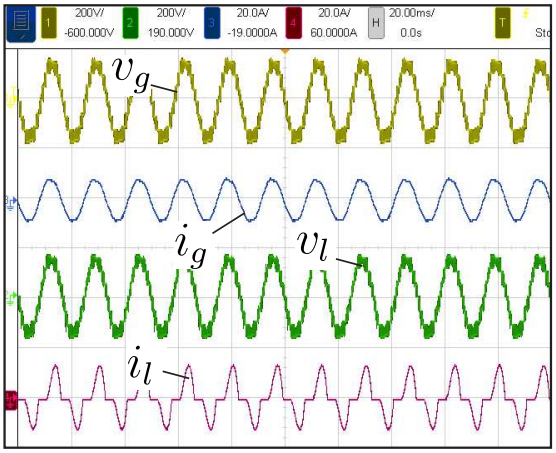
Fig. 2.16 demonstrates the shunt compensation capability of the proposed system. For this test, the 5L-HFL operated with the nonlinear load presented in Fig. 2.7. Fig. 2.16(a) shows a load transient due to a load power increase of about 45%. Fig. 2.16(b)-(c) show the behavior of the dc-link voltages and grid and load currents with zoomed views before and after the transient, respectively. The proposed system ensured harmonic and reactive currents compensation and dc-link voltages regulation.

The same experimental tests were done for $\eta = 3$. From top to bottom, Fig. 2.17(a) shows the grid voltage (e_g) and current (i_g) in phase, as well as the shunt compensation current (i_s) and the load current (i_l). From top to bottom, Fig. 2.17(b) depicts the voltage generated by the shunt (v_g) and series (v_l) sides with nine levels. Then, Fig. 2.17(c) shows the voltages (v_{pT}, v_{sT}) and currents (i_{pT}, i_{sT}) at the primary and secondary windings of the HFT. Fig. 2.18 validates the operation of the proposed configuration under 20% of grid voltage sag. One can see that the load voltage e_l and the dc-link voltages remain controlled. Lastly, Fig. 2.19 demonstrates the shunt compensation capability of the proposed system. Fig. 2.19(a) depict a load power increase of 45%. Fig. 2.19(b)-(c) depict the behavior of the dc-link voltages and grid and load currents with zoomed views before and after the transient, respectively. Notice that the proposed system ensured harmonic and reactive currents compensation and dc-link voltages regulation for $\eta = 3$.

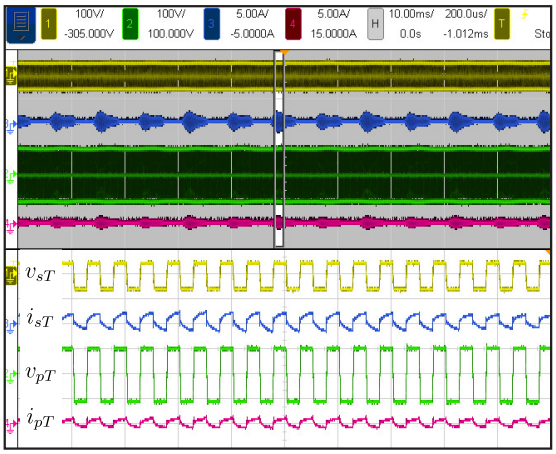
Figure 2.14 – Experimental results in steady state for $\eta = 2$. (a) Grid voltage (e_g), grid current (i_g), shunt compensation current (i_s), and load current (i_l). (b) Shunt and series converter voltage (v_g and v_l). (c) Voltages (v_{pT}, v_{sT}) and currents (i_{pT}, i_{sT}) in the primary and secondary side of the transformer.



(a)

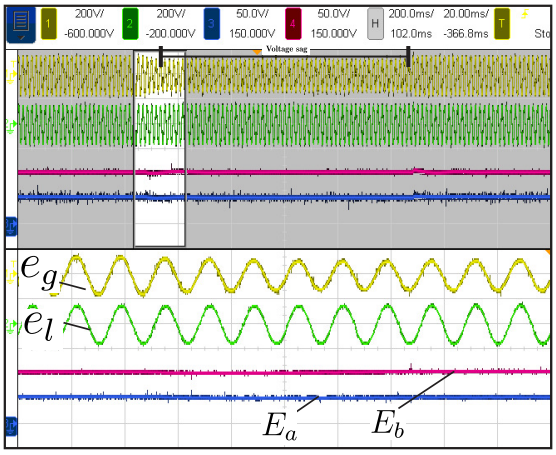


(b)

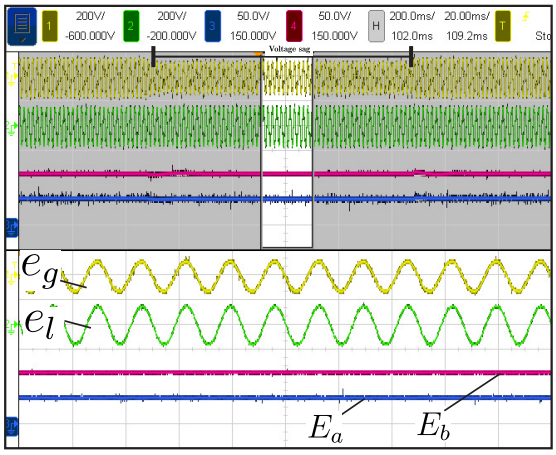


(c)

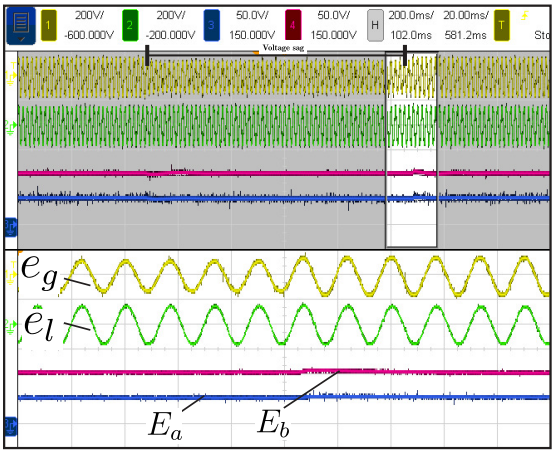
Figure 2.15 – Experimental results with a linear load under 20% of grid voltage sag for $\eta = 2$. (a) Dc-link voltages (E_a and E_b) and Grid (e_g) and load (e_l) voltages with zoomed view in the beginning of the disturbance. (b) Dc-link voltages (E_a and E_b) and Grid (e_g) and load (e_l) voltages with zoomed view during the disturbance. (c) Dc-link voltages (E_a and E_b) and Grid (e_g) and load (e_l) voltages with zoomed view in the end of the disturbance.



(a)

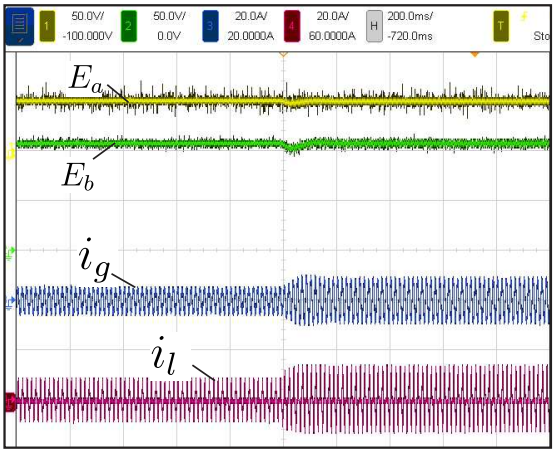


(b)

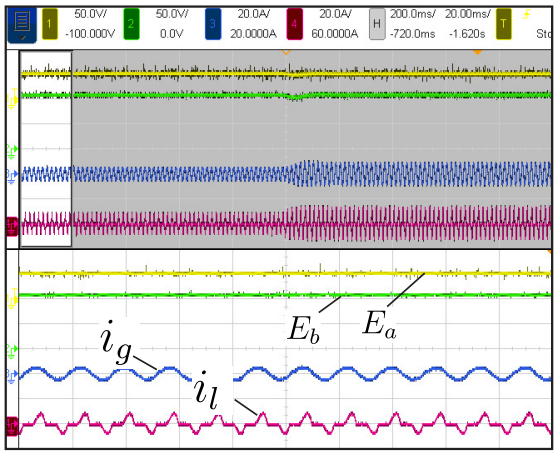


(c)

Figure 2.16 – Experimental results with a nonlinear load for $\eta = 2$. (a) Dc-link voltages (E_a and E_b) and grid (i_g) and load (i_l) currents. (b) Dc-link voltages (E_a and E_b) and grid (i_g) and load (i_l) currents with zoomed view before the disturbance. (c) Dc-link voltages (E_a and E_b) and grid (i_g) and load (i_l) currents with zoomed view after the disturbance.



(a)



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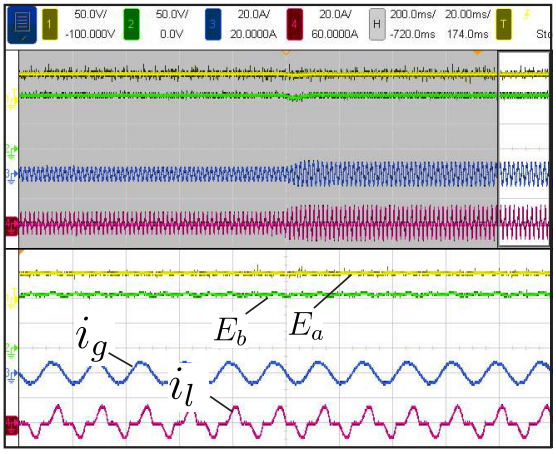
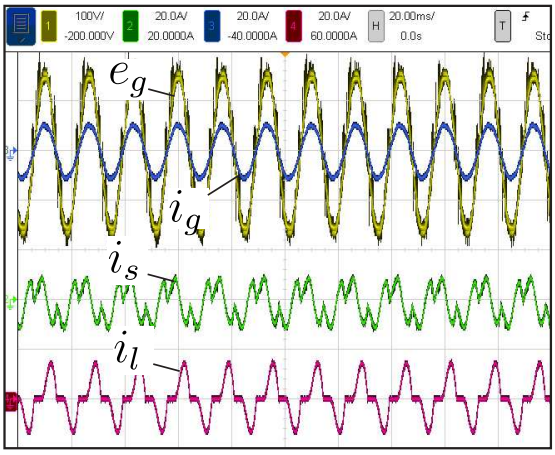
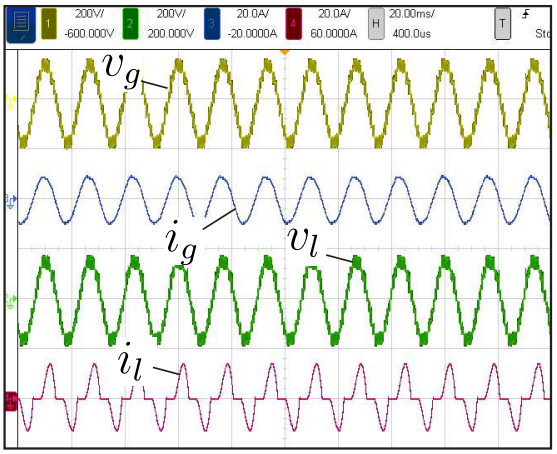


(c)

Figure 2.17 – Experimental results in steady state for $\eta = 3$. (a) Grid voltage (e_g), grid current (i_g), shunt compensation current (i_s), and load current (i_l). (b) Shunt and series converter voltage (v_g and v_l). (c) Voltages (v_{pT}, v_{sT}) and currents (i_{pT}, i_{sT}) in the primary and secondary side of the transformer.



(a)



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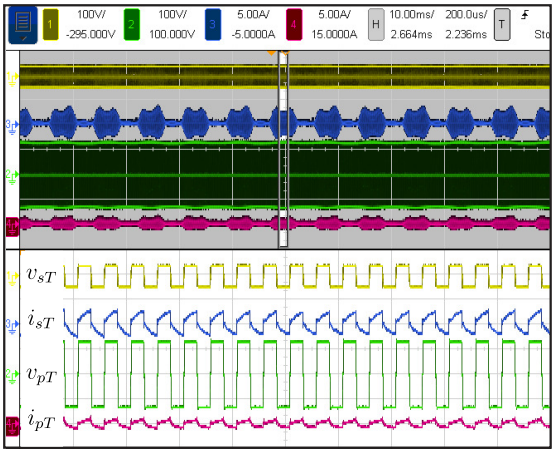
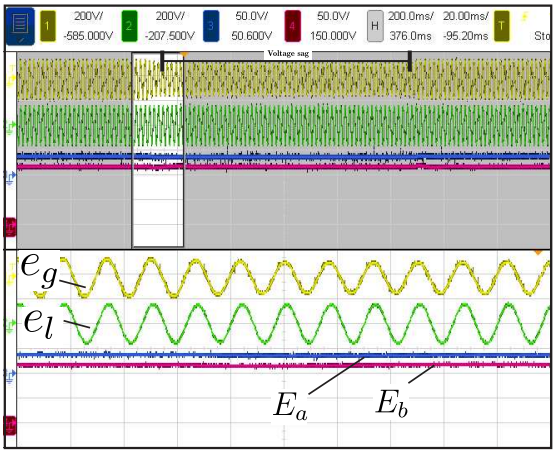
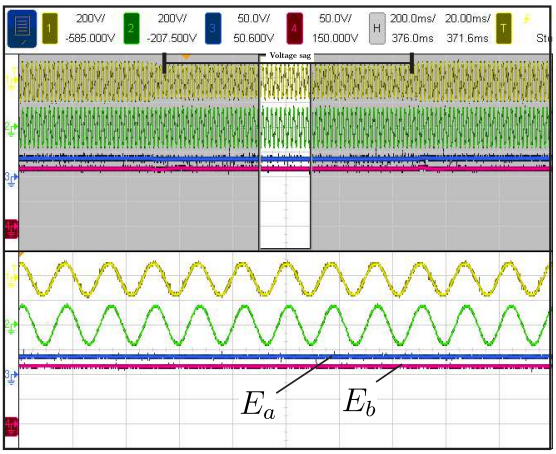


(c)

Figure 2.18 – Experimental results with a linear load under 20% of grid voltage sag for $\eta = 3$. (a) Dc-link voltages (E_a and E_b) and Grid (e_g) and load (e_l) voltages with zoomed view in the beginning of the disturbance. (b) Dc-link voltages (E_a and E_b) and Grid (e_g) and load (e_l) voltages with zoomed view during the disturbance. (c) Dc-link voltages (E_a and E_b) and Grid (e_g) and load (e_l) voltages with zoomed view in the end of the disturbance.



(a)



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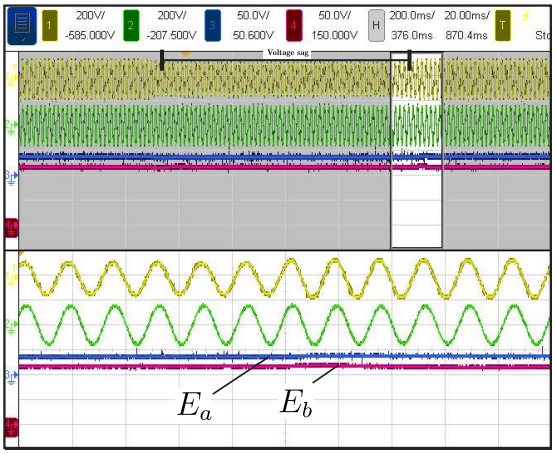
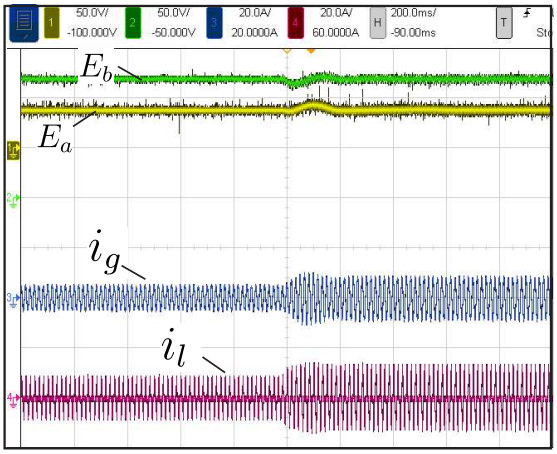
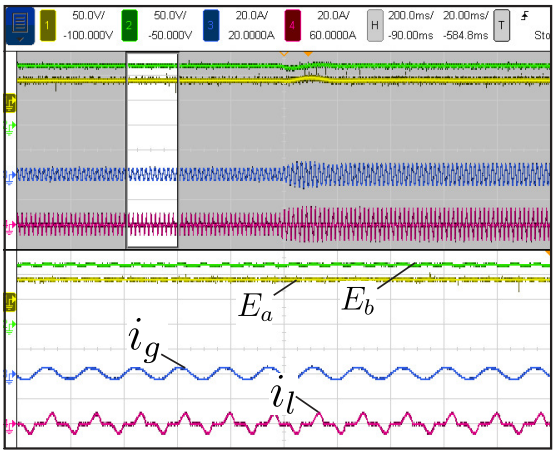


(c)

Figure 2.19 – Experimental results with a nonlinear load for $\eta = 3$. (a) Dc-link voltages (E_a and E_b) and grid (i_g) and load (i_l) currents. (b) Dc-link voltages (E_a and E_b) and grid (i_g) and load (i_l) currents with zoomed view before the disturbance. (c) Dc-link voltages (E_a and E_b) and grid (i_g) and load (i_l) currents with zoomed view after the disturbance.



(a)



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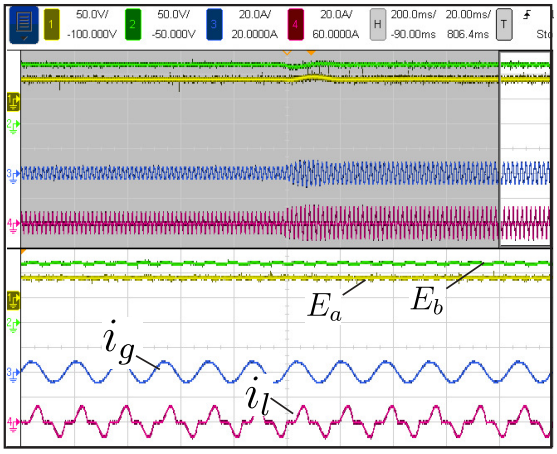
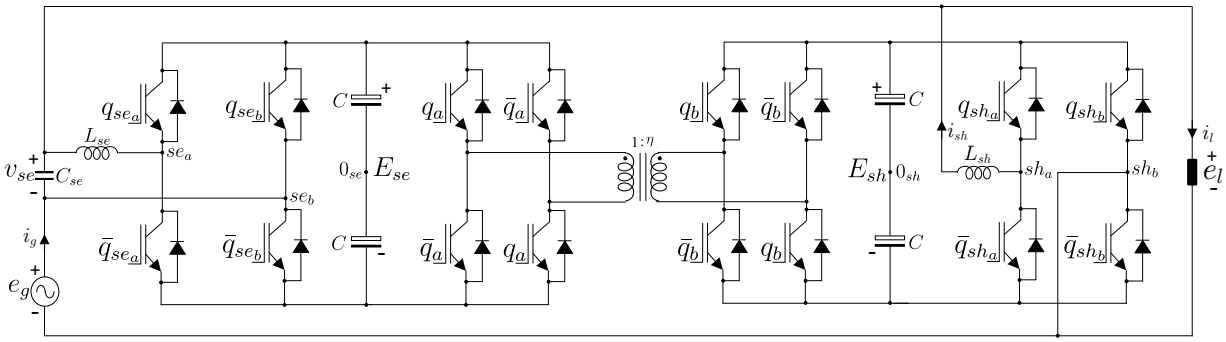


(c)

2.7 Comparison of the Topologies

For fair comparisons, the 4L-HFL UPQC topology (PEREDA; DIXON, 2011), presented in Fig. 2.20, was selected, since it employs an HFL and it has similarities in terms of the number of semiconductors when compared with 5L-HFL converter. This analysis takes into account harmonic distortion, power losses, and ac-filter size. Unless made clear otherwise, the parameters used in tests for both studied topologies are addressed in Table 2.3.

Figure 2.20 – 4L-HFL Converter (PEREDA; DIXON, 2011).



2.7.1 Harmonic Distortion Analysis

The weighted total harmonic distortion (WTHD) of shunt and series voltages and the total harmonic distortion (THD) of the grid and load currents are calculated to compare the conventional and proposed converters. From (HOLMES; LIPO, 2003), the WTHD and THD can be calculated, respectively, by

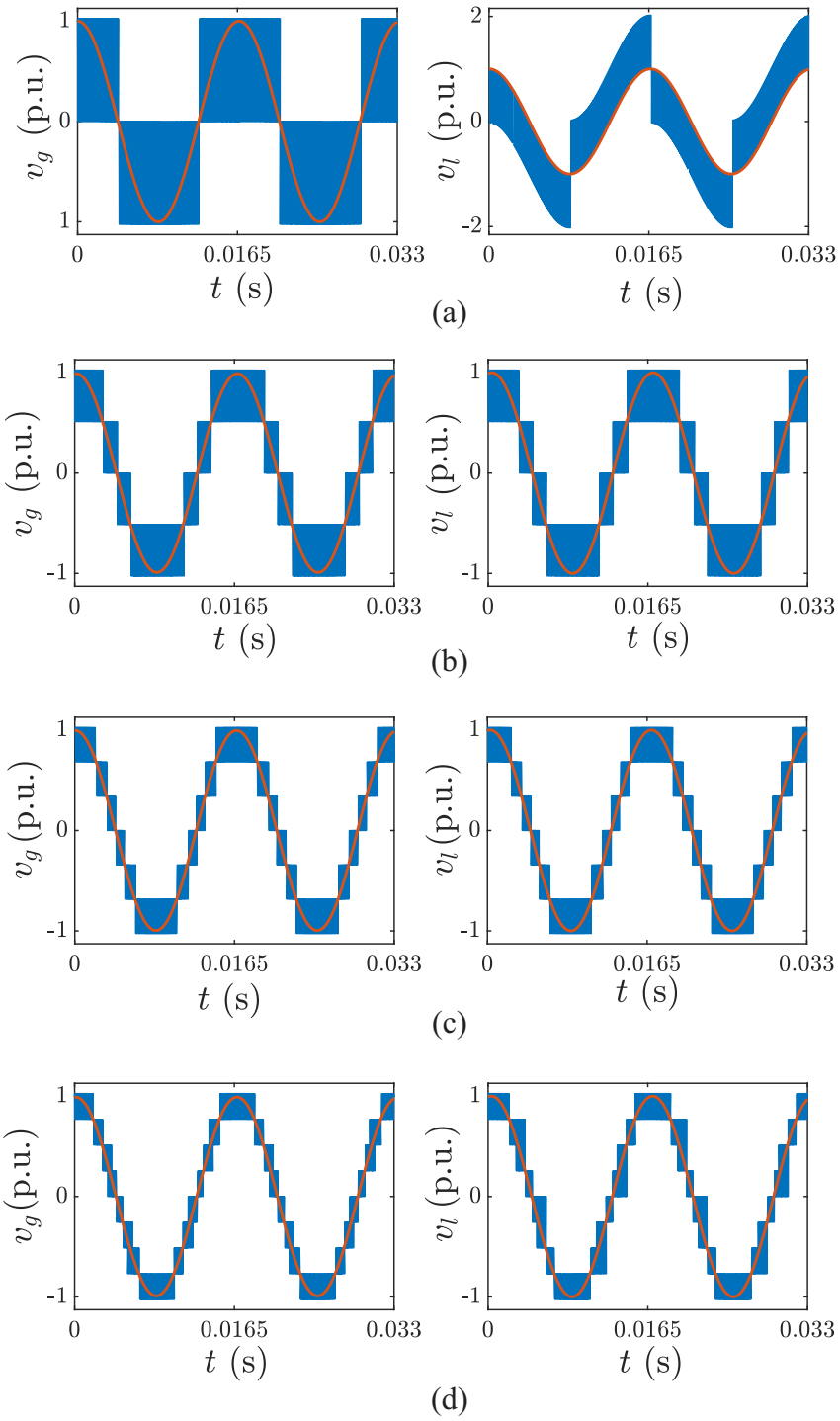
$$WTHD(\%) = \frac{100}{\gamma_1}\sqrt{\sum_{n=2}^{N_h}\left(\frac{\gamma_n}{n}\right)^2}, \tag{2.21}$$

$$THD(\%) = \frac{100}{\gamma_1}\sqrt{\sum_{n=2}^{N_h}\gamma_n^2}, \tag{2.22}$$

where γ_1 is the amplitude of the fundamental component, γ_n is the amplitude of the harmonic of order n, and N_h is the number of harmonics that are used in the calculation. The WTHD and THD values were calculated considering $Nh = 100$ components.

Table 2.7 shows the WTHD and THD values, and Fig. 2.21 shows the shunt and series voltages generated by the 4L-HFL and 5L-HFL converters under rated conditions. For the 4L-HFL converter, v_g is defined by the voltage generated by the shunt module, and v_l is determined by the grid voltage and the voltage synthesized by the series module, disregarding the passive filter composed by the inductance L_{se} and the capacitance C_{se}. In this way, one can write $v_g = v_{sh_a 0_{sh}} - v_{sh_b 0_{sh}}$ and $v_l = e_g - (v_{se_a 0_{se}} - v_{se_b 0_{se}})$.

Figure 2.21 – Voltages v_g and v_l generate by 5L-HFL and 4L-HFL. (a) 4L-HFL. (b) 5L-HFL - $E_b = E_a$ ($\eta = 1$). (c) 5L-HFL - $E_b = 2E_a$ ($\eta = 2$). (d) 5L-HFL - $E_b = 3E_a$ ($\eta = 3$).



As expected, the proposed topology exhibited the lowest harmonic content due to the higher number of levels generated on the shunt and series sides and, consequently, the current ripple with lower di/dt. Table 2.7 also shows the percentage reduction (PR(%)) of the 5L-HFL converter compared to the 4L-HFL converter in terms of the WTHD values of the voltage and the THD values of the current. Considering $\eta = 3$, the proposed structure achieves 76% improvement in the shunt voltage WTHD value and 56% improvement in

the series voltage WTHD value compared to the conventional converter. Lower harmonic content may result in better converter efficiency and the ac-filter size reduction, as addressed in the following sections.

Table 2.7 – Voltage WTHD (%) and current THD (%) values.

Converter	η	WTHD (%)		THD (%)		PR (%) WTHD (%)		THD (%)	
		v_g	v_l	i_g	i_l	v_g	v_l	i_g	i_l
4L-HFL	$\eta = 1$	0.30	0.16	4.88	0.33	-	-	-	-
5L-HFL	$\eta = 1$	0.13	0.14	2.20	0.32	56.6	12.5	54.9	3.03
	$\eta = 2$	0.09	0.09	1.87	0.25	70.0	43.7	61.6	24.2
	$\eta = 3$	0.07	0.09	1.65	0.26	76.6	43.7	66.1	21.2

2.7.2 Power Losses Analysis

Semiconductor power losses were determined using the thermal modules. The switching power modules selected for analysis were IGBT SKM50GB063D from Semikron. The conduction (P_{cd}), switching (P_{sw}), and total power losses ($P_{tot} = P_{cd} + P_{sw}$) were calculated by setting the THD value of the grid current in 5%, which was obtained by adjusting the PWM sampling frequency of the main converter (shunt and series modules). The sampling frequency of the main converter for 4L-HFL and 5L-HFL is given in Table 2.8. The HFL sampling frequency was kept at 10 kHz for all power losses analysis.

Table 2.8 – Power Losses Evaluation for THD(i_g) = 5%.

Converter	η	f_s (kHz)	P_{cd} (W)		P_{sw} (W)		P_{tot} (W)	PR(%)
			main	HFL	main	HFL		P_{tot}
4L-HFL	$\eta = 1$	10.0	22.30	0.20	19.17	12.56	54.2	-
5L-HFL	$\eta = 1$	4.2	36.60	1.85	7.73	4.72	51.0	5.90
	$\eta = 2$	3.5	35.36	1.55	3.79	4.46	45.2	16.6
	$\eta = 3$	3.0	32.76	1.52	3.33	4.47	42.1	22.3

$*$ Considering THD (i_g) = 5%.

As can be seen, the proposed topology presents higher conduction losses because it has more power switches than the conventional converter. Nevertheless, 5L-HFL achieved lower switching losses since it presents lower voltage stress on the power switches and operates with lower dv/dt than 4L-HFL. Therefore, observing the total power losses, the decrease in the switching losses on the proposed configuration compensates the increase in the conduction losses. According to Table 2.8, the PR(%) in the total semiconductor power losses for 5L-HFL corresponds to 5.7%, 16.6%, and 22.3% compared to 4L-HFL in scenarios with η = 1, 2, and 3, respectively.

2.7.3 AC-Filter Design

This section details the design of the ac-filters L_g, L_l, and C_l, considering the maximum current ripple of the grid and load currents. As shown in (LANGE et al., 2015), the minimum inductance of the grid current filter is

$$L_{g_{\min}} = \frac{\Delta V}{4 f_s \Delta i_{g_{\max}}}, \tag{2.23}$$

where $\Delta i_{g_{max}}$ is the maximum current ripple required in the design, and ΔV is the amplitude of each voltage level over the grid inductor. For the proposed topology, ΔV depends on the transformer turn ratio η. Then, (2.23) can be rewritten for any η value as

$$L_{g_{\min}} = \frac{E^*}{4 f_s \Delta i_{g_{\max}} (1+\eta)}. \tag{2.24}$$

Notice that, for the same system parameters design and considering $\eta = 3$, the grid inductance of 5L-HFL presents a percentage reduction in the size of up to 75% compared to 4L-HFL. The minimum load inductance $L_{l_{\min}}$ can be calculated in the same way. More details about the inductor filter design can be found in Appendix A.

The expression for the capacitance can be determined by considering that the resonance frequency (f_r) of the filter should be much lower than the sampling frequency and much higher than the line frequency to avoid harmonics from the converter and grid. After calculating f_r, the filter capacitance, C_l, is determined using the resonance frequency expression

$$C_l = \frac{1}{(2\pi f_r)^2 L_l}. \tag{2.25}$$

2.8 High-Frequency Link

As already mentioned, a SAB converter based on HFT is used to process the energy between the two dc links. For each aforementioned scenario of dc-link voltage ratio, the transformer turn ratio η can be defined as $\eta = \eta_p/\eta_s$, where η_p and η_s are the numbers of turns required by the primary and secondary sides, respectively. Since the active bridge of the SAB converter produces a square-wave with a constant duty cycle and sampling frequency $f_t = 1/T_t$, the following equation can be derived

$$v_{pT}(t) = \begin{cases} \frac{\eta E}{1+\eta}, & 0 < t < \frac{T_t}{2} \\ -\frac{\eta E}{1+\eta}, & \frac{T_t}{2} < t < T_t. \end{cases} \tag{2.26}$$

Taking into account a triangular magnetic flux (ϕ) in the toroidal core, it can be written

$$\phi(t) = \begin{cases} \frac{4\phi_{\max}}{T_t}t - \phi_{\max}, \ 0 < t < \frac{T_t}{2} \\ -\frac{4\phi_{\max}}{T_t}t + 3\phi_{\max}, \ \frac{T_t}{2} < t < T_t, \end{cases} \tag{2.27}$$

$$v_{pT}(t) = \eta_p \frac{\phi(t)}{dt} = \begin{cases} \eta_p \frac{4\phi_{\max}}{T_t}, \ 0 < t < \frac{T_t}{2} \\ -\eta_p \frac{4\phi_{\max}}{T_t}, \ \frac{T_t}{2} < t < T_t. \end{cases} \tag{2.28}$$

Considering (2.26) and (2.28) as well as $\phi_{\max} = AB_{\max}$, the number of turns in the primary winding can be written as

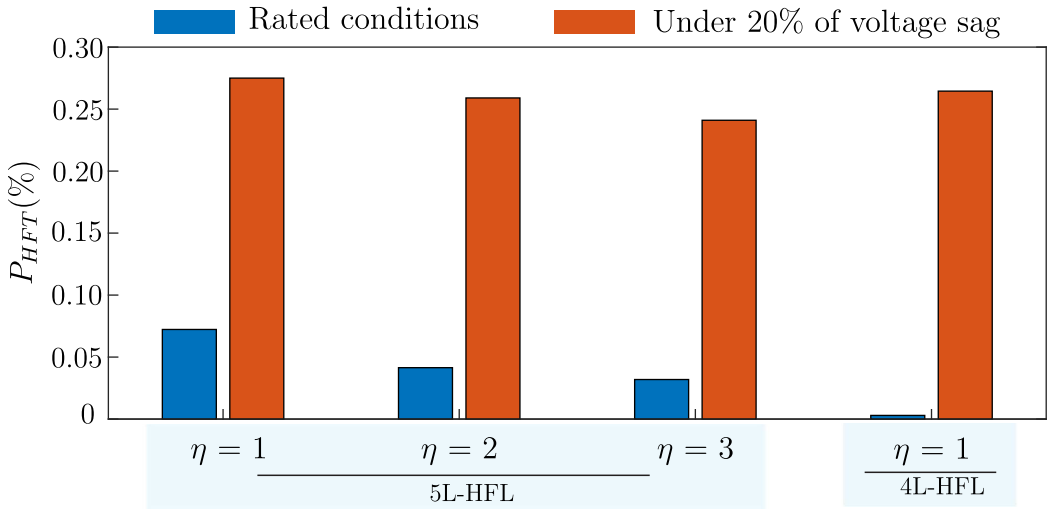
$$n_p = \frac{\eta E}{4 f_t A B_{\max}(1+\eta)}, \tag{2.29}$$

where A is the core area, $B_{\max}$ is the flux density, and η can be selected for any dc-link voltage ratio presented in Table 2.1. Due to high-frequency operation, the transformer has low weight and volume. In addition, the HFL is connected through the shared path of the circuit, which has a lower current amplitude than the grid and the load paths for a wide range of inductive and capacitive loads. Fig. 2.22 presents the power processed by the HFL in the proposed and conventional structures during rated and grid voltage sag conditions. For $\eta = 1$, 2, and 3 the HFL in the proposed converter process, respectively, only 7.22%, 4.14%, and 3.19% of the rated load power during rated conditions, demonstrating low power consumption. When operating with 20% of grid voltage, the transformer's power reaches up to 27% of the rated power when $\eta = 1$. In the conventional converter, the series module and, consequently, the HFL does not process power in rated conditions. Nevertheless, in scenarios with 20% of grid voltage sag, the HFL reaches 26.45% over the rated load power.

2.9 Conclusion

In this Chapter, it was investigated a single-phase ac-dc-ac converter based on an HFT. The topology consists of a tree-leg module with a series connected full-bridge converter to the shared part of the system and an HFL interfacing the two dc links. The system model, PWM strategy, and control scheme were presented. In addition, a power distribution analysis was performed to define the operating ranges in which the dc-link voltages can be controlled without additional voltage and current sensors. In this context, the proposed control system is more simplified when compared to the conventional solution with floating capacitors. On the other hand, the phase angle limits between the shunt (v_g) and series (v_l) converter voltages must be respected to ensure proper operation. It has been noticed that the space-vector plane becomes narrower when η increases.

Figure 2.22 – Processed power in the HFL for 5L-HFL and 4L-HFL.



Although the 5L-HFL converter has more semiconductor devices (one more fast diode module), the HFL allowed asymmetrical dc-link voltages operation with high modulation index, which improved the overall performance of the proposed configuration in terms of harmonic distortion and power losses. Furthermore, since the HFL consists of a SAB converter, it requires fewer controlled switches, fewer isolated gate drivers, and a simplified control strategy compared to the DAB converter.

The comparative analysis showed that the proposed 5L-HFL converter has lower total power losses than 4L-HFL, which were reduced by 5.7%, 16.6%, and 22.3% in scenarios with $\eta = 1$, 2, and 3, respectively. In addition, in terms of ac-filter size, the proposed converter offers up to 75% size reduction compared to the 4L-HFL converter because it can generate multilevel waveforms on the grid and load sides. Moreover, the experimental tests have shown that the proposed system ensures the compensation of the grid power factor, the regulation of the dc-link voltages, and grid sag mitigation.

Chapter 3

PUC Converter Based on AC-DC-AC Multilevel Topology with a Shared Leg

3.1 Introduction

Nowadays, due to the expansion of power demand from residential, commercial, and industrial customers, PQ problems become more frequent and critical (RAUF et al., 2016). The widespread use of electronic equipment increases the number of disturbances in the power grid, such as voltage sags and swells, harmonic voltages and currents, flicker, and spikes (KHADKIKAR et al., 2006; NIELSEN; BLAABJERG, 2005). To mitigate these problems, one may use power conditioning equipment such as the UPQC systems that can provide both series and shunt compensation, simultaneously (FUJITA; AKAGI, 1998; KHADKIKAR, 2012).

The full-bridge UPQC, presented in Fig. 1.2 and named here 4L, is the conventional single-phase ac-dc-ac UPQC topology. This topology is composed by two h-bridge voltage source inverters, a line-frequency transformer, and a dc-link capacitor interfacing series and shunt units. Different UPQC topologies have already been proposed (KHADKIKAR, 2012; NASIRI; EMADI, 2003). Several UPQC topologies and related control strategies were reviewed in (KHADKIKAR, 2012). It is worth pointing out that for single-phase low-cost low-power applications the three-leg UPQC and half-bridge UPQC are the most popular ones (NASIRI; EMADI, 2003). Both configurations demand less semiconductor power switches in comparison to the 4L converter.

To provide power quality, multilevel converters have been employed in UPQC topologies. In (RODRIGUES et al., 2019), two single-phase ac-dc-ac four-leg converters

with a low-frequency transformer were studied. These converter topologies can provide a better performance in terms of harmonic distortion when compared to the conventional four-leg converter. In (LACERDA et al., 2020), a series connected six-leg converter with a low-frequency transformer has been proposed. Although such a six-leg converter has more power switches than the 4L converter, it provides more voltage levels for the grid and load sides. In (HAN et al., 2006), a UPQC based on several pairs of four-leg modules has been proposed. In this case, a multiwinding transformer allows to connect the shunt unit to yield multilevel waveforms at the output. In (GAUTAM; YADAV; GUPTA, 2012), a topology based on three-leg modules connected to series/parallel arrangements has been investigated. In this study, a single-phase ac-dc-ac converter composed of two three-leg modules parallel-connected to the rectifier side and a series connected to the inverter side was proposed. In (FREITAS et al., 2019), a single-phase ac-dc-ac converter with a series connection composed by a transformer and two three-leg modules has been investigated. This topology brings advantages regarding voltage stress on the power switches and number of voltage levels.

Given the advantages of converter structures that exploit multilevel features, in this Chapter, a single-phase ac-dc-ac multilevel configuration based on packed u-cell (PUC) is investigated. The system consists of a four-leg module with a u-cell connected to the shared part of the system and a low-frequency transformer at the grid side. A u-cell comprises two switches and one dc link. The first converter based on u-cells was introduced in (OUNEJJAR; AL-HADDAD; GREGOIRE, 2011). This solution has less capacitors and power switches than the cascaded h-bridge converter (CHB), neutral point-clamped converter (NPC), and flying capacitor converter (FC). The proposed converter allows one to compensate for grid voltage sags and swells, and to provide a high power factor at the grid side with low harmonic content. Besides, the proposed converter can operate with minimum dc-link voltage values in applications in which the grid and load frequency are the same, such as unified power quality conditioners (UPQC). The proposed configuration is compared to the conventional single-phase four-leg UPQC regarding the amount of power processed by the transformer, rating of semiconductor devices, harmonic distortion, ac-filter size, and semiconductor power losses. The system model, the operational constraints, the power distribution analysis, the overall control system strategy, and a space vector pulse-width modulation that exploits a simplified carrier-based approach are presented. Simulation and experimental results are addressed to confirm the feasibility of the proposed converter as well as the correctness of the design methodology.

3.2 System Model

This section details the proposed topology in terms of its equivalent circuit, dc-link voltage specifications, operating regions, and synchronization.

Figure 3.1 – Proposed ac-dc-ac configuration.

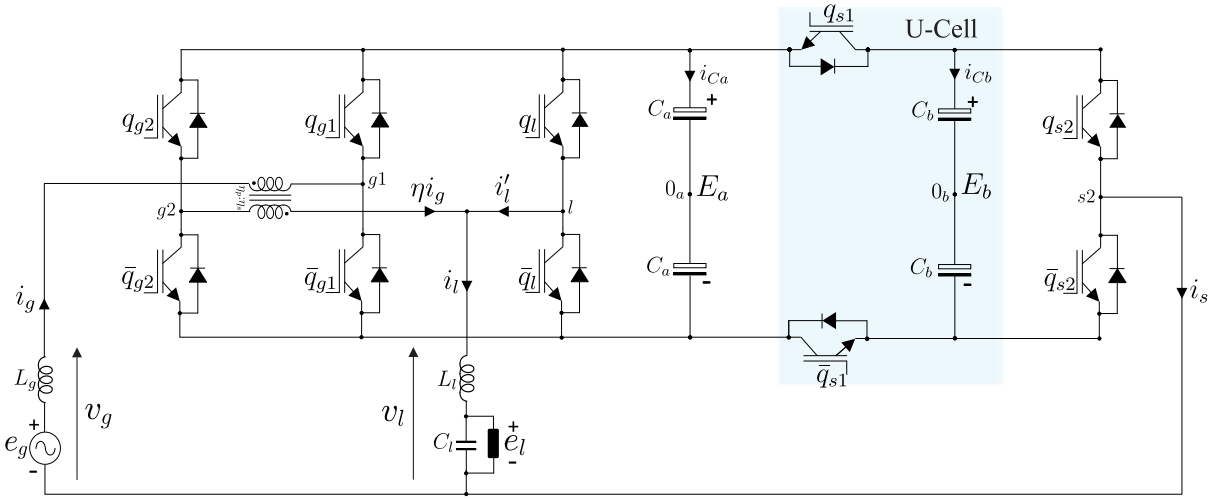
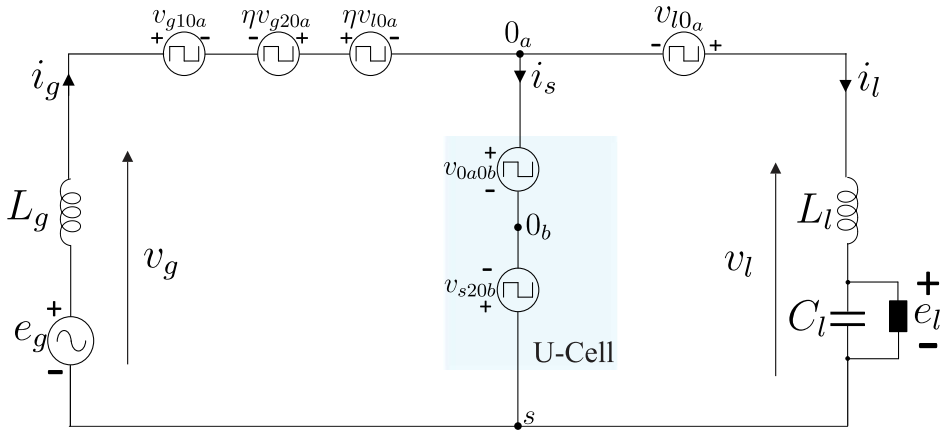


Figure 3.2 – Equivalent circuit.



3.2.1 Circuit Description

The proposed system is constituted of two dc-links (C_a and C_b), four two-level legs, and a u-cell, as shown in Fig. 3.1. Furthermore, this configuration is fed by a single-phase grid with voltage and current given by e_g and i_g, respectively, and supplies a load with voltage and current defined by e_l and i_l. The converter is composed of switches $q_k - \bar{q}_k$, with $k = \{g1,\ g2,\ l,\ s1,\ s2\}$. Pairs $q_k - \bar{q}_k$ are complementary and the switching conduction state is represented by $q_k = 1$ when the switch is closed and $q_k = 0$ when is opened.

Fig. 3.2 presents the equivalent circuit model to the 4L-PUC. For the circuit analysis, the transformer is considered ideal and the turn ratio of the transformer is defined as $\eta = \eta_p/\eta_s$. Applying Kirchhoff's voltage and current laws the following equations can be derived

$$e_g = v_g + Z_g i_g, \tag{3.1}$$

$$e_l = v_l - Z_l i_l, \tag{3.2}$$

$$i_s = i_g - i_l, \tag{3.3}$$

where v_g and v_l are the shunt and series converter voltages, respectively, while i_s is the shunt compensation current and $Z_g = r_g + \frac{d}{dt} l_g$ and $Z_l = r_l + \frac{d}{dt} l_l$ represent the impedance of inductors L_g and L_l, respectively. The shunt and series voltage, v_g and v_l, can be calculated from the converter pole voltages as

$$v_g = v_{g10a} + v_{0a0b} - v_{s0b} + \eta(v_{l0a} - v_{g20a}), \tag{3.4}$$

$$v_l = v_{l0a} + v_{0a0b} - v_{s0b}. \tag{3.5}$$

The pole voltages v_{g10a}, v_{g20a}, v_{l0a}, and v_{s20b} can be generically denoted by

$$v_{j0m} = (2q_j - 1)\frac{E_m}{2}, \tag{3.6}$$

where E_m is the dc-link voltage of the converter with $m = \{a, b\}$, and q_j represents the binary state of the top switches with $j = \{g1, g2, l\}$ when $m = a$, and with $j = \{s2\}$ when $m = b$. The pole voltage v_{0a0b} is obtained by taking into account the voltage between the dc-link midpoints 0_a and 0_b, as follows

$$v_{0a0b} = (2q_{s1} - 1)\left(\frac{E_b - E_a}{2}\right). \tag{3.7}$$

3.2.2 Dc-link Voltage Specifications

From this point on the symbol * denotes a reference variable. To ensure that v_g and v_l are synthesized correctly, the following conditions must be considered for 4L-PUC converter considering the maximums e minimums pole voltage values

$$|v_g^*| \leq E_b^* + \eta E_a^*, \tag{3.8}$$

$$|v_l^*| \leq E_b^*, \tag{3.9}$$

$$|v_g^* - v_l^*| \leq \eta E_a^*. \tag{3.10}$$

For equally spaced input and output voltage levels, to reduce harmonic distortion, it was chosen that the dc-link voltage ratio is $E_b = 2E_a$. Considering (3.8)-(3.10), the minimum dc-links voltage values for 4L-PUC are given by

$$E^*_{a_{\min}} = \max\left\{\frac{|v^*_g|}{1/2+\eta}, \frac{|v^*_l|}{2}, \frac{|v^*_g - v^*_l|}{\eta}\right\}, \tag{3.11}$$

$$E^*_{b_{\min}} = \max\left\{\frac{|v^*_g|}{1+\eta/2}, |v^*_l|, \frac{|v^*_g - v^*_l|}{\eta/2}\right\}. \tag{3.12}$$

3.2.3 Operational Constraints

Depending on the values of η, it is possible to choose relationships between the amplitudes values of the grid (E_g) and load (V_l) voltages to maximize the number of levels synthesized by the proposed converter or to make it more efficient. Table 3.1 presents the operational constraints for 4L and 4L-PUC converters taking into account the amplitudes of v_g and v_l equal to 1 p.u. (rated conditions). V_{swell} and V_{sag} are, respectively, the maximum grid voltage swell and sag supported considering the minimum dc-link voltage value; N_{lvl_g} and N_{lvl_l} are the numbers of levels generated by v_g and v_l. The 4L and 4L-PUC converters can operate in three different scenarios of transformer turn ratio. For 4L topology, the operation with multilevel features, only in the grid side, occurs for $\eta = 2$ and $\eta = 3$. The 4L-PUC converter can synthesize multilevel waveforms in the grid and load sides when operating with $\eta = 1$ or $\eta = 1/2$. In any scenario, both converters can deal with a percentage of grid voltage sag and swell. In this way, the transformer turn ratio selected to analyze in this work takes into account the compromise between a reasonable range to compensate voltage disturbances in the fundamental frequency, as well as, the generation of waveforms with low harmonic content. Therefore, it was selected $\eta = 2$ for 4L configuration and $\eta = 1$ for 4L-PUC converter.

Table 3.1 – Characteristics of 4L and 4L-PUC Configurations According To the Transformer Turn Ratio.

Converter	η	$V_g = V_l = 1$ p.u.			
		V_{swell}	V_{sag}	N_{lvl_g}	N_{lvl_l}
4L	1	1.0	1.0	3	3
	2	0.50	0.50	5	3
	3	0.33	0.33	7	3
4L-PUC	2	1.0	0.50	3	5
	1	0.50	0.50	5	5
	1/2	0.25	0.25	9	5

3.2.4 Synchronization

Since $\mathbf{V}_g = V_g\angle\varphi_g$ and $\mathbf{V}_l = V_l\angle(\varphi_g+\varepsilon)$, to operate with minimum dc-link voltages values, the phase angle between v_g and v_l (ε) must respect (3.8)-(3.10) for 4L-PUC. Table

3.2 shows the phase angle limits between v_g and v_l for 4L and 4L-PUC under rated conditions, 50% of grid voltage sag, and 50% of grid voltage swell. Notice that, both configurations can deal with 50% of sag or swell.

Table 3.2 – Phase Angle Limits Between v_g and v_l.

Converter	η	Operation	ε
4L	2	rated condition	$\lvert\varepsilon\rvert \leq 28.95°$
		50% of sag	$\varepsilon = 0°$
		50% of swell	$\varepsilon = 0°$
4L-PUC	1	rated condition	$\lvert\varepsilon\rvert \leq 28.95°$
		50% of sag	$\varepsilon = 0°$
		50% of swell	$\varepsilon = 0°$

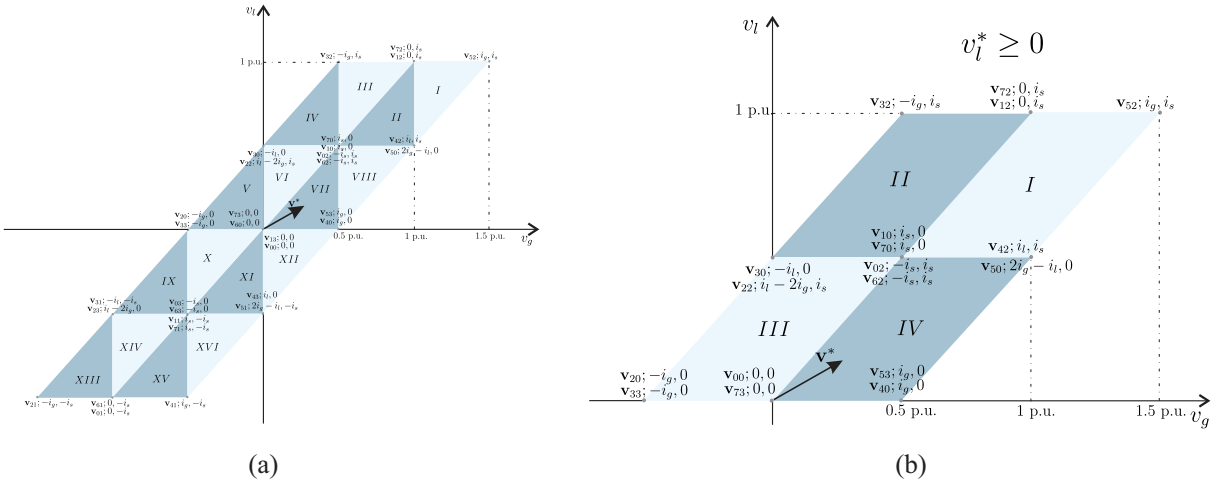


Figure 3.3 – Space-vector plan for 4L-PUC converter ($\eta = 1$). (a) Complete space-vector plan; (b) Simplified space-vector plan.

3.3 PWM Techniques

In this section, a space-vector pulse-width modulation (SV-PWM) and a carrier-based PWM are developed. Fig. 3.3(a) presents the space-vector plane of topology 4L-PUC considering $E_b = 2E_a = 1$ p.u. and $\eta = 1$. Each vertex represents a vector and each triangle is a sector ($K = I, II, III, ..., XVI$). The voltage vectors are defined by a sequence of switching states. For the proposed configuration, the sequence is represented as $\mathbf{v}_{n_a n_b}$, where n_a and n_b are the binary sequences $\{q_{g1}, q_{g2}, q_l\}$ and $\{q_{s1}, q_{s2}\}$, respectively, converted to decimal numbers. Thus, consider that ($\mathbf{v}_{n_a n_b}$; i_{Ca}, i_{Cb}) represents the switching states of a voltage vector and the respective current through the dc-link capacitors C_a (i_{Ca}) and C_b (i_{Cb}), respectively.

Considering the coordinates in the vector plane, a voltage vector is denoted by $\mathbf{v}_{n_a n_b} = v_g + \mathrm{j}v_l$, where v_g and v_l are the real (Re) and imaginary (Im) parts of the vector

$\mathbf{v}_{n_a n_b}$, respectively. In the SV-PWM technique, the reference voltage, $\mathbf{v}^*_{n_a n_b} = v^*_g + \mathrm{j}v^*_l$, is synthesized by the three closest vectors. These vectors are defined as $\mathbf{v}_a$, $\mathbf{v}_b$, and $\mathbf{v}_c$. Considering $\mathbf{v}^*_{n_a n_b}$ constant during a sampling period T, it can be written that

$$\mathbf{v}^*_{n_a n_b} = \tau_a \mathbf{v}_a + \tau_a \mathbf{v}_b + \tau_a \mathbf{v}_c, \tag{3.13}$$

where τ_a, τ_b, and τ_c represent the duty cycles of the vectors $\mathbf{v}_a$, $\mathbf{v}_b$, and $\mathbf{v}_c$, respectively. The duty cycle of each vector can be determined by

$$\begin{bmatrix} \tau_a \\ \tau_b \\ \tau_c \end{bmatrix} = \begin{bmatrix} \mathrm{Re}(\mathbf{v}_a) & \mathrm{Re}(\mathbf{v}_b) & \mathrm{Re}(\mathbf{v}_c) \\ \mathrm{Im}(\mathbf{v}_a) & \mathrm{Im}(\mathbf{v}_b) & \mathrm{Im}(\mathbf{v}_c) \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} v^*_g \\ v^*_l \\ 1 \end{bmatrix}. \tag{3.14}$$

As can be seen in Fig. 3.3(a), there are some possibilities for selecting the three vectors to produce the reference vector $\mathbf{v}^*_{n_a n_b}$. For example, the voltage vector $\mathbf{v}_{n_a n_b} = 0.5 + \mathrm{j}0.5$, can be synthesized by $\mathbf{v}_{70}$, $\mathbf{v}_{10}$, $\mathbf{v}_{02}$, and $\mathbf{v}_{62}$. These redundancies may be chosen to either reduce the average switching frequency or regulate a dc-link voltage.

Taking into account the redundant vectors, an equivalent carrier-based PWM can be also introduced. Considering v^*_g and v^*_l as the desire reference voltages, the reference pole voltages can be rewritten from (3.4) and (3.5) as

$$v^*_{g10a} + v^*_{0a0b} - v^*_{s0b} + v^*_{l0a} - v^*_{g20a} = v^*_g, \tag{3.15}$$

$$v^*_{l0a} + v^*_{0a0b} - v^*_{s0b} = v^*_l. \tag{3.16}$$

Since v^*_g and v^*_l are provided by the shunt and series control, respectively, all the reference pole voltage values can be determined if at least three of them are known. Choosing, for example, the sector $K = I$ in Fig. 3.3(a), the vectors which best reduce the switching losses are defined by the sequence $\mathbf{v}_{72}$-$\mathbf{v}_{52}$-$\mathbf{v}_{42}$. Observing this sequence, v^*_{g10a}, v^*_{0a0b}, and v^*_{s20b} are constant over a sampling period, while v^*_{g20a} and v^*_{l0a} can be determined by combining (15) and (16). This approach was applied to the other sectors, in which adjacent sectors with the same reference pole voltages were associated, producing the space-vector plan shown in Fig. 3.3(b). Another simplification was made by considering the space-vector plane symmetry for v^*_l. For example, the vector $\mathbf{v}_{70}$ ($\mathbf{v}_{n_a n_b} = 0.5 + \mathrm{j}0.5$) is complementary to vector $\mathbf{v}_{03}$ ($\mathbf{v}_{n_a n_b} = -0.5 - \mathrm{j}0.5$). In this way, the space-vector plane can be simplified from 16 to 4 sectors ($K' = I, II, III,$ and IV).

To reduce switching losses, the reference pole voltages can be calculated for each sector of K' considering $v^*_l \geq 0$ and $E_a = E_b/2 = E$ as follows

$$\text{if } K' = I,\ v^*_{g10a} = \frac{E}{2}, v^*_{0a0b} = \frac{E}{2}, v^*_{s20b} = -E,$$
$$v^*_{g20a} = v^*_l - v^*_g + \frac{E}{2}, v^*_{l0a} = v^*_l - \frac{3E}{2} \quad (3.17)$$

$$\text{if } K' = II,\ v^*_{g10a} = -\frac{E}{2}, v^*_{0a0b} = \frac{E}{2}, v^*_{s20b} = -E,$$
$$v^*_{g20a} = v^*_l - v^*_g - \frac{E}{2}, v^*_{l0a} = v^*_l - \frac{3E}{2} \quad (3.18)$$

$$\text{if } K' = III,\ v^*_{g10a} = -\frac{E}{2}, v^*_{l0a} = -\frac{E}{2}, v^*_{s20b} = -E,$$
$$v^*_{g20a} = v^*_l - v^*_g - \frac{E}{2}, v^*_{0a0b} = v^*_l - \frac{E}{2} \quad (3.19)$$

$$\text{if } K' = IV,\ v^*_{g10a} = \frac{E}{2}, v^*_{l0a} = -\frac{E}{2}, v^*_{s20b} = -E,$$
$$v^*_{g20a} = v^*_l - v^*_g + \frac{E}{2}, v^*_{0a0b} = v^*_l - \frac{E}{2} \quad (3.20)$$

Using carrier-based PWM, the gating signals for each switch can be achieved by comparing the reference pole voltages with only one high-frequency triangular carrier signal as presented in Fig. 3.4.

Figure 3.4 – Carrier-based PWM.

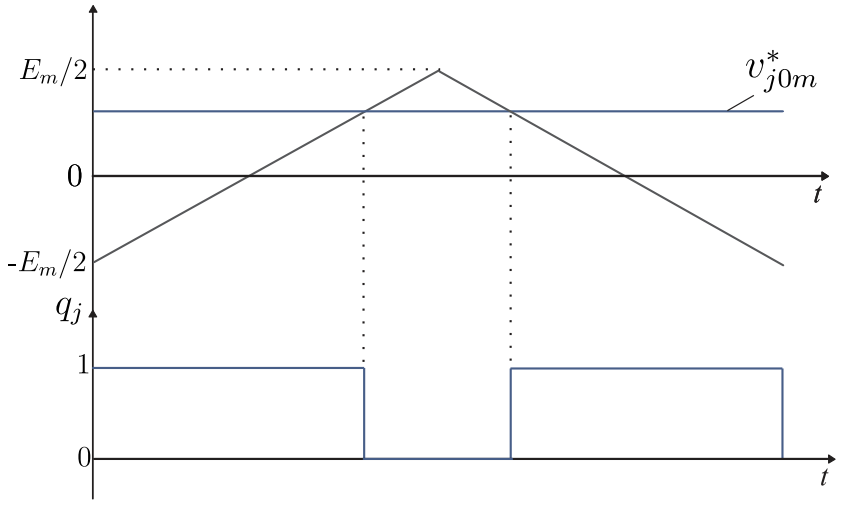


Table 3.3 – Selected vector sequences and calculated reference pole voltage to charge or discharge dc-link voltage E_a for $\eta = 1$.

Operation mode sq_1/sq_2	Sector K'	Sector K	Vector Sequence $\mathbf{v}_a \Rightarrow \mathbf{v}_b \Rightarrow \mathbf{v}_c$	v^*_{g10a}	v^*_{g20a}	v^*_{l0a}	v^*_{0a0b}	v^*_{s20b}
$(i_s \geq 0 \ \& \ \mu'^* = 0)$	I	I	$\mathbf{v}_{72} \Rightarrow \mathbf{v}_{52} \Rightarrow \mathbf{v}_{42}$	$\frac{E}{2}$	v^*_l-v^*_g+$\frac{E}{2}$	v^*_l-$\frac{3E}{2}$	$\frac{E}{2}$	-E
		II	$\mathbf{v}_{72} \Rightarrow \mathbf{v}_{62} \Rightarrow \mathbf{v}_{42}$					
	II	III	$\mathbf{v}_{32} \Rightarrow \mathbf{v}_{12} \Rightarrow \mathbf{v}_{02}$	-$\frac{E}{2}$	v^*_l-v^*_g-$\frac{E}{2}$	v^*_l-$\frac{3E}{2}$	$\frac{E}{2}$	-E
		IV	$\mathbf{v}_{32} \Rightarrow \mathbf{v}_{22} \Rightarrow \mathbf{v}_{02}$					
||	III	V	$\mathbf{v}_{22} \Rightarrow \mathbf{v}_{20} \Rightarrow \mathbf{v}_{00}$	-$\frac{E}{2}$	v^*_l-v^*_g-$\frac{E}{2}$	-$\frac{E}{2}$	v^*_l-$\frac{E}{2}$	-E
		VI	$\mathbf{v}_{22} \Rightarrow \mathbf{v}_{02} \Rightarrow \mathbf{v}_{00}$					
$(i_s < 0 \ \& \ \mu'^* = 1)$	IV	VII	$\mathbf{v}_{62} \Rightarrow \mathbf{v}_{60} \Rightarrow \mathbf{v}_{40}$	$\frac{E}{2}$	v^*_l-v^*_g+$\frac{E}{2}$	-$\frac{E}{2}$	v^*_l-$\frac{E}{2}$	-E
		VIII	$\mathbf{v}_{62} \Rightarrow \mathbf{v}_{42} \Rightarrow \mathbf{v}_{40}$					
$(i_s \geq 0 \ \& \ \mu'^* = 1)$	I	I	$\mathbf{v}_{72} \Rightarrow \mathbf{v}_{52} \Rightarrow \mathbf{v}_{50}$	$\frac{E}{2}$	v^*_l-v^*_g+$\frac{E}{2}$	$\frac{E}{2}$	v^*_l-$\frac{3E}{2}$	-E
		II	$\mathbf{v}_{72} \Rightarrow \mathbf{v}_{70} \Rightarrow \mathbf{v}_{50}$					
	II	III	$\mathbf{v}_{32} \Rightarrow \mathbf{v}_{12} \Rightarrow \mathbf{v}_{10}$	-$\frac{E}{2}$	v^*_l-v^*_g-$\frac{E}{2}$	$\frac{E}{2}$	v^*_l-$\frac{3E}{2}$	-E
		IV	$\mathbf{v}_{32} \Rightarrow \mathbf{v}_{30} \Rightarrow \mathbf{v}_{10}$					
||	III	V	$\mathbf{v}_{30} \Rightarrow \mathbf{v}_{20} \Rightarrow \mathbf{v}_{00}$	-$\frac{E}{2}$	v^*_l-v^*_g-$\frac{E}{2}$	v^*_l-$\frac{E}{2}$	-$\frac{E}{2}$	-E
		VI	$\mathbf{v}_{30} \Rightarrow \mathbf{v}_{10} \Rightarrow \mathbf{v}_{00}$					
$(i_s < 0 \ \& \ \mu'^* = 0)$	IV	VII	$\mathbf{v}_{70} \Rightarrow \mathbf{v}_{60} \Rightarrow \mathbf{v}_{40}$	$\frac{E}{2}$	v^*_l-v^*_g+$\frac{E}{2}$	v^*_l-$\frac{E}{2}$	-$\frac{E}{2}$	-E
		VIII	$\mathbf{v}_{70} \Rightarrow \mathbf{v}_{50} \Rightarrow \mathbf{v}_{40}$					

3.4 Control System

In this section, the control strategy for the proposed converter is discussed, including the shunt and series control, as well as, the dc-link voltages regulation.

3.4.1 Overall Control Strategy

The control diagram of configuration 4L-PUC is shown in Fig. 3.5(a). Firstly, the average value of the dc-link voltage $E_m = \frac{E_a+E_b}{2}$ is regulated by a conventional PI controller $[R_{E_m}(s) = K_{pE} + \frac{K_{iE}}{s}]$, which gives the amplitude of the grid reference current I_g^*. To generate the reference grid current, i_g^*, synchronized with the fundamental frequency of the grid voltage e_g, a single-phase phase-locked loop (PLL) approach is used to obtain the phase angle of the grid voltage (δ_g). A resonant controller R_{i_g}, presented in (JACOBINA et al., 2001), is implemented to define the shunt reference voltage v_g^*. Its transfer function is given by

$$R_{i_g}(s) = 2\frac{K_{p_{i_g}} s^2 + K_{i_{i_g}} s}{s^2 + \omega^2}, \tag{3.21}$$

where $\omega = 2\pi f$ and f is the fundamental grid frequency.

The series control is also implemented using a resonant controller as described in (3.21). The resonant controller sets the series reference voltage, v_l^*, taking into account the amplitude of the load reference voltage E_l^* and its phase angle ε.

3.4.2 Dc-link voltage balancing

Since the proposed converter has two dc-link voltages, one of then needs to be controlled individually. For this purpose, a conventional PI controller represented by the R_{E_a} block $[R_{E_a}(s) = K_{pE_a} + \frac{K_{iE_a}}{s}]$ is implemented to regulate the dc-link voltage E_a. Then, saturation/comparator block, named SC_μ, is used to provide a binary variable $\mu'^* = \{0, 1\}$. In this way, it has been defined that if $\mu'^* = 1$, the dc link must be charged. Meanwhile, if $\mu'^* = 0$, the dc link must be discharged.

To define the sequences of the PWM to adjust the dc link voltage E_a, the sequence of vectors must be taken into account, because redundant voltage vectors have different capacitor-current contributions. The currents through the dc-link capacitor C_a is given by

$$i_{Ca} = i_g[q_{g1} + \eta(q_l - q_{g2})] - i_l q_l - i_s q_{s1}. \tag{3.22}$$

As can be seen, i_{Ca} depends on the choice of the switching state. Observing Fig. 3.3(b), the voltage vector 0.5 + j0.5 can be generated by either $\mathbf{v}_{10}$, $\mathbf{v}_{70}$, $\mathbf{v}_{02}$, or $\mathbf{v}_{62}$. When $\mathbf{v}_{10}$ is applied, $i_{Ca} = i_s$ and, when $\mathbf{v}_{02}$ is used i_{Ca} = -i_s. The same is valid for $\mathbf{v}_{70}$ and $\mathbf{v}_{62}$, respectively. Therefore, the redundant voltage can be used to regulate the dc-link voltage.

The technique to regulate E_a is described in flowchart form in Fig. 3.5(b). The sequence of vectors chosen (sq_1 or sq_2) considers the polarity of the shunt compensation current and the binary variable μ'^*, which determines whether the dc link needs to be charged or discharged. Table 3.3 summarizes the best sequence of vectors that minimize switching losses and the calculated reference pole voltages for each sector K and K' of the space-vector plan. Notice that, the reference pole voltages v^*_{g10a} and v^*_{s20b} are always constant over a sampling period, indicating that they operate at low frequency.

3.4.3 Power flow analysis

Neglecting the converter power losses, the processing power over 4L-PUC converter can be determined as

$$p_{in} - p_{out} = p_{Ca} + p_{Cb}, \tag{3.23}$$

where p_{in} and p_{out} are the input and output power of the converter, respectively, while p_{Ca} and p_{Cb} are the power in the dc-links C_a and C_b, respectively. Since $p_{in} = v_g i_g$ and $p_{out} = v_l i_l$, (3.23) can be rewritten as

$$v_g i_g - v_l i_l = p_{Ca} + p_{Cb}, \tag{3.24}$$

and thus,

$$[v_{g10a} + v_{0a0b} - v_{s20b} + \eta(v_{l0a} - v_{g20a})]i_g - (v_{l0a} + v_{0a0b} - v_{s20b})i_l = p_{Ca} + p_{Cb}. \tag{3.25}$$

From (3.25), it is possible to define p_{Ca} as follows

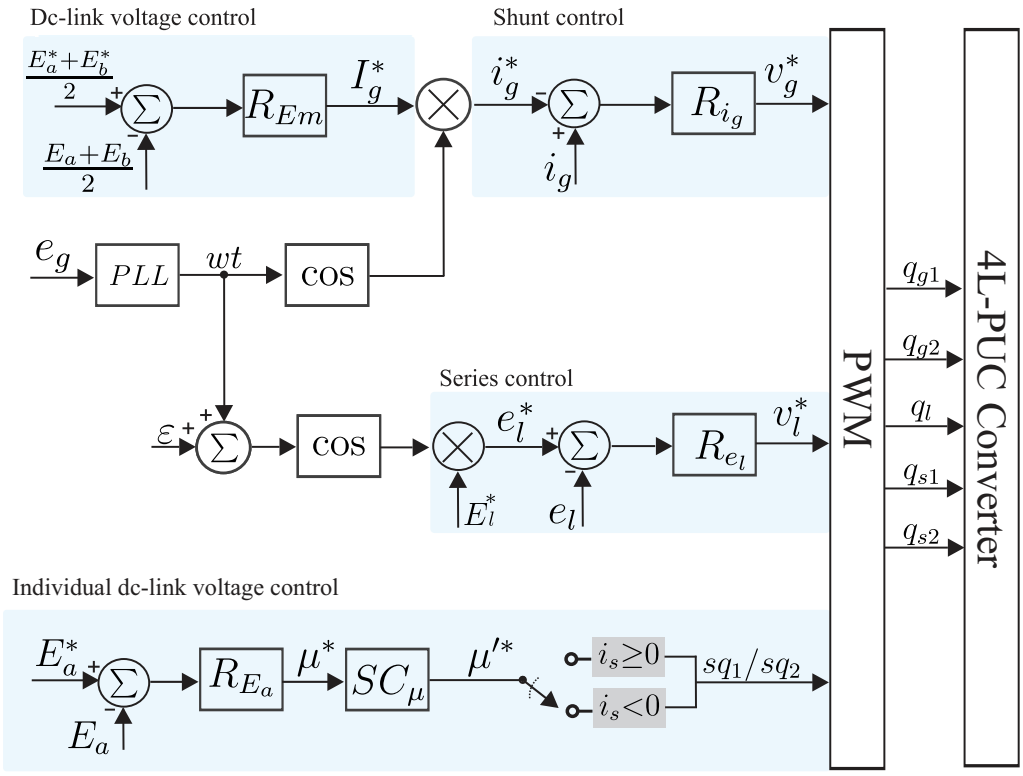
$$p_{Ca} = [v_{g10a} + \eta(v_{l0a} - v_{g20a})]i_g - v_{l0a}i_l - v_{0a}i_s, \tag{3.26}$$

where $v_{0a} = [(2q_{s1} - 1)\frac{-E_a}{2}]$ corresponds to the portion referring to the dc-link voltage E_a in (3.7).

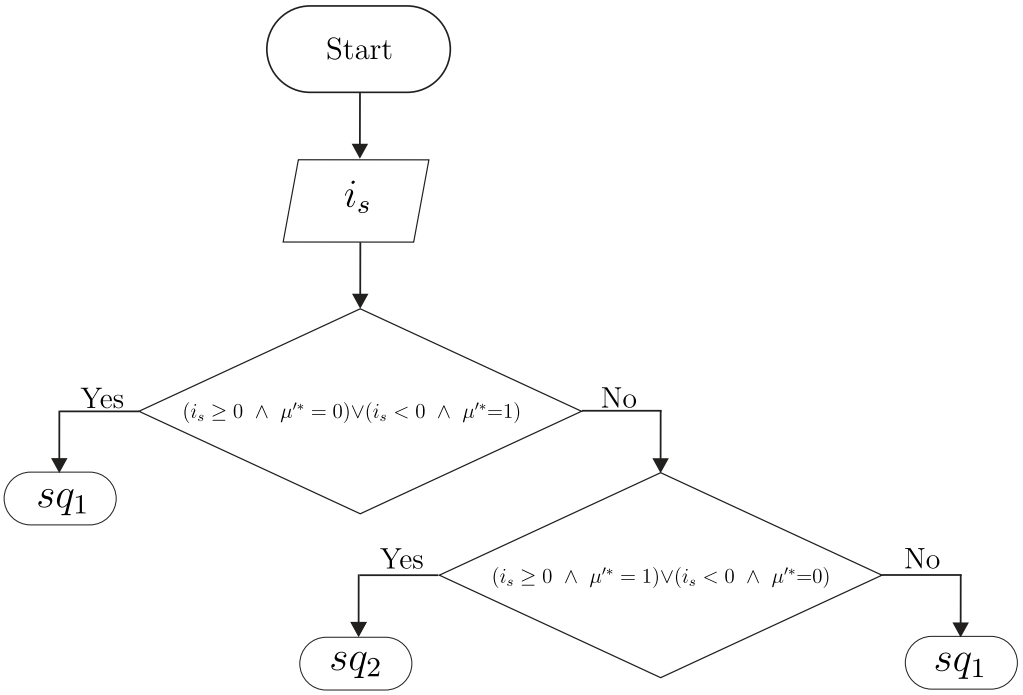
From (3.26), steady-state simulations were performed to verify the operations constraints of the dc-link voltage regulation taking into account a variation in the amplitude of the grid voltage from $E_g = 0.5$ to 1.5 and the load power factor from $\cos(\gamma_l) = 0.6$ to 1, series voltage amplitude $V_l = 311$ V, frequency of the triangular carrier $f_s = 10$ kHz, and load power $P_l = 1$ kW. The steady-state system voltage and currents are given by $\mathbf{E}_g = E_g\angle\delta_g$, $\mathbf{V}_g = V_g\angle(\delta_g + \varphi_g)$, $\mathbf{I}_g = I_g\angle\delta_g$, $\mathbf{V}_l = V_l\angle(\delta_g + \varepsilon)$, and $\mathbf{I}_l = I_l\angle(\delta_g + \varepsilon + \delta_l)$.

Fig. 3.6 presents the power distribution of p_{Ca} when the dc-link voltage E_a is set to charge [Fig. 3.6(a)] or discharge [Fig. 3.6(b)]. The dc-link voltage balance is ensured when p_{Ca} returns positive values if commanded to charge and negative values if commanded to discharge. Observing these graphs, the 4L-PUC converter can handle voltage sags and

Figure 3.5 – Overall control system. (a) Control diagram. (b) Flowchart for individual dc-link voltage balancing.



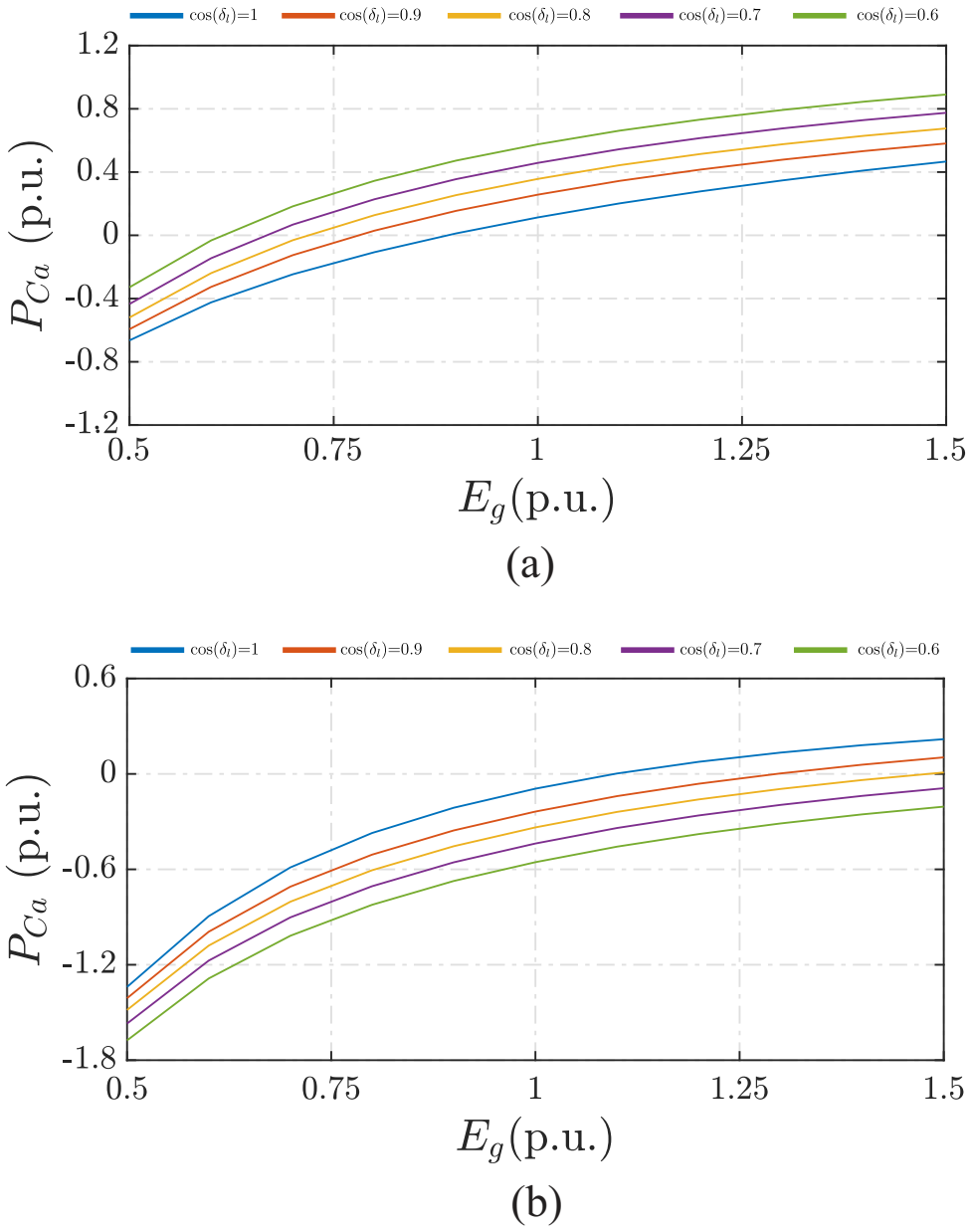
(a)



(b)

swells for a wide range of load power factors. The main constraints are related to the performance with a unitary load power factor. In this case, the operation is limited to $0.86 \leq E_g \leq 1.11$. On the other hand, this range can be extended by operating with a lower modulation index value.

Figure 3.6 – The power distribution of the dc-link voltage E_a as a function of the amplitude of the grid voltage for $\eta = 1$. (a) Operation constraints when E_a is selected to charge. (b) Operation constraints when E_a is selected to discharge.



3.5 Results

To demonstrate the feasibility of the proposed converter, simulation and experimental results in closed-loop control are presented. The setup utilized during the experiment

is presented in Fig. 3.7. Semiconductor power devices from SEMIKRON, with IGBTs and gate drivers SKHI22, as well as, a DSP TMS320F28335 from Texas Instruments$^{\text{ő}}$ it was used. Unless made clear otherwise, Table 3.4 shows the parameters used in the simulation and experimental for the proposed configuration.

Table 3.4 – Parameters used in simulations and experimental tests.

Parameter		Value
Grid voltage	e_g	220 V rms (Case 1) 176 V rms (Case 2) 264 V rms (Case 3)
Load reference voltage	e_l^*	220 V rms
Transformer turn ratio	η	1
Switching frequency	f_s	10 kHz
Dc-link capacitors	C_a, C_b	4.7 mF
Grid inductance	L_g	5 mH
RL Load		
Load power factor	$\cos(\delta_l)$	0.788 (lagging)
Load filter inductance	L_l	2 mH
Load filter capacitance	C_l	18 μH
Nonlinear load I		
Dc-link voltage	E_a, E_b	170/340 V
Apparent power	S_l	5.5 kVA
Load current THD	THD_{il}	70%
Nonlinear load II		
Dc-link voltage	E_a, E_b	170/340 V
Apparent power	S_l	2.03 kVA
Load current THD	THD_{il}	58%

3.5.1 Simulation Results

Simulation results have been performed to demonstrate the capability of the proposed system to compensate harmonic and reactive current, as well as, grid voltage harmonics, sags and swells, ensuring shunt and series compensation. Firstly, Figs. 3.8, 3.9, and 3.10 present the capability of the proposed system to compensate simultaneously for grid voltage and load current disturbances for the three cases of operation: rated, sag, and swell conditions. For all three scenarios mentioned, the grid voltage is composed by 10%, 5%, and 2% of third, fifth and seventh harmonics, respectively. Also, the converter feeds a nonlinear load formed by a single-phase unidirectional rectifier (Nonlinear load I). Notice that for all scenerios of operation the proposed system ensures series and shunt compensation.

Figure 3.7 – Experimental setup used in the tests. 1 - Grid; 2 - Load: nonlinear load + RL load; 3 - Grid inductance; 4 - Transformer; 5 - Voltage and current sensors; 6 - 4L-PUC; 7 - Drivers; 8 - Oscilloscope; 9 - Voltmeters.

Then, the capability of the proposed control system to compensate transients with grid voltage sags and swells has been demonstrated in Fig. 3.11 and 3.12, respectively by applying 20% of disturbance at the moment $t = 3$ s. In this case, the 4L-PUC feeding a RL load. As can be seen, in both cases the load voltage e_l and dc-link voltages remain regulated in their reference value. Besides, the grid current is kept controlled.

Fig. 3.13 shows the system performance when is applied a step in the load power by about 27% when there is a grid voltage sag of 20%. In this test, it was considered as load a single-phase rectifier to produce harmonic content (Nonlinear load II). It can be noticed that the dc-link voltages remain controlled and the amplitude of the load voltage is kept constant. Furthermore, the grid power factor control is ensured.

Figure 3.8 – Simulation results of the proposed converter operating with grid voltage and load current disturbances under rated conditions. (a) Grid voltage (with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic) and grid current. (b) Load current and shunt compensation current. (c) Dc-link voltages E_a. (d) Dc-link voltages E_b. (e) Packed u-cell (PUC) voltage (v_0s2). (f) Pole voltage v_{0a0b}.(g) Shunt converter voltage. (g) Series converter voltage.

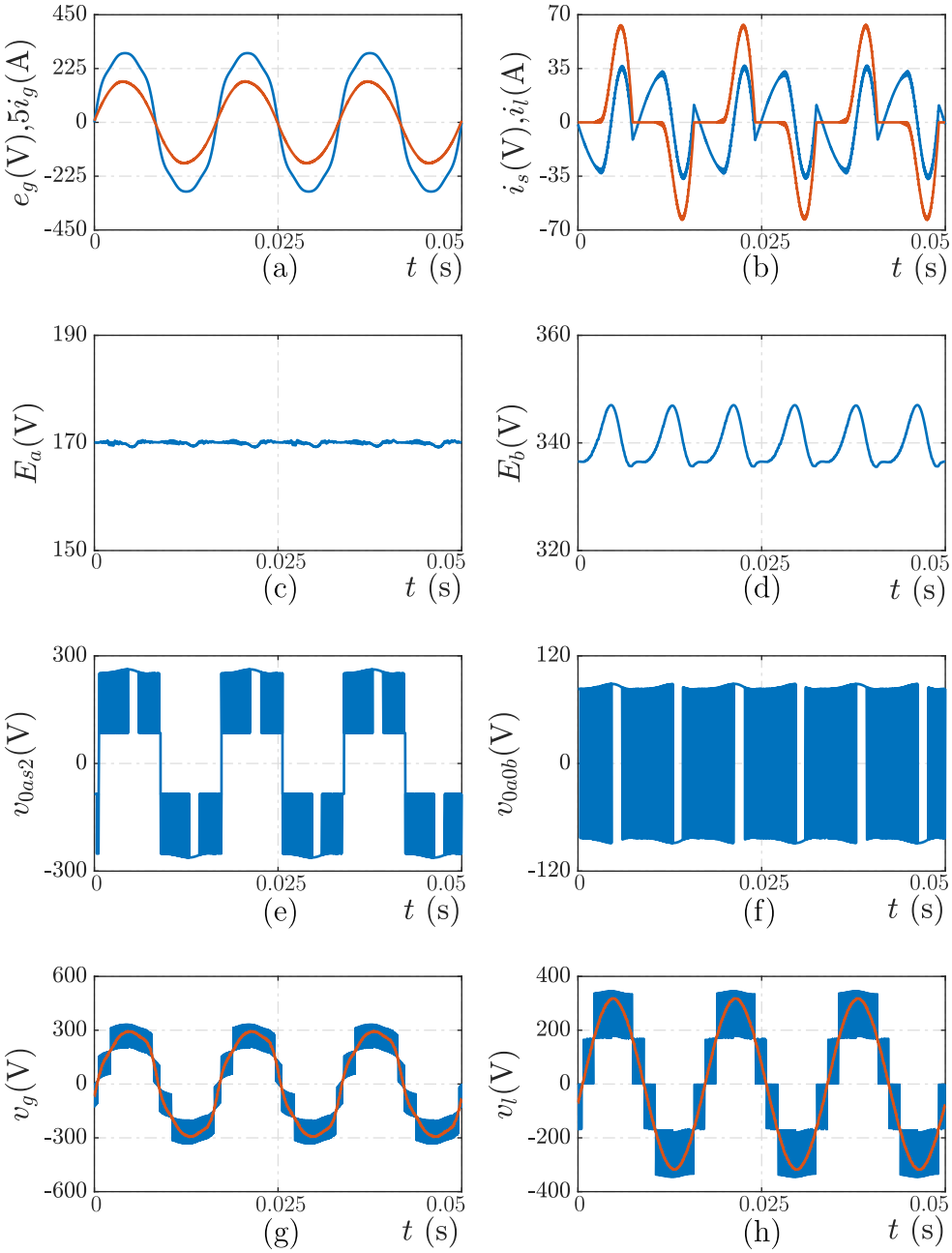


Figure 3.9 – Simulation results of the proposed converter operating with grid voltage and load current disturbances 30% of grid voltage sag. (a) Grid voltage (with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic) and grid current. (b) Load current and shunt compensation current. (c) Dc-link voltages E_a. (d) Dc-link voltages E_b. (e) Packed u-cell (PUC) voltage (v_0s2). (f) Pole voltage v_{0a0b}.(g) Shunt converter voltage. (g) Series converter voltage.

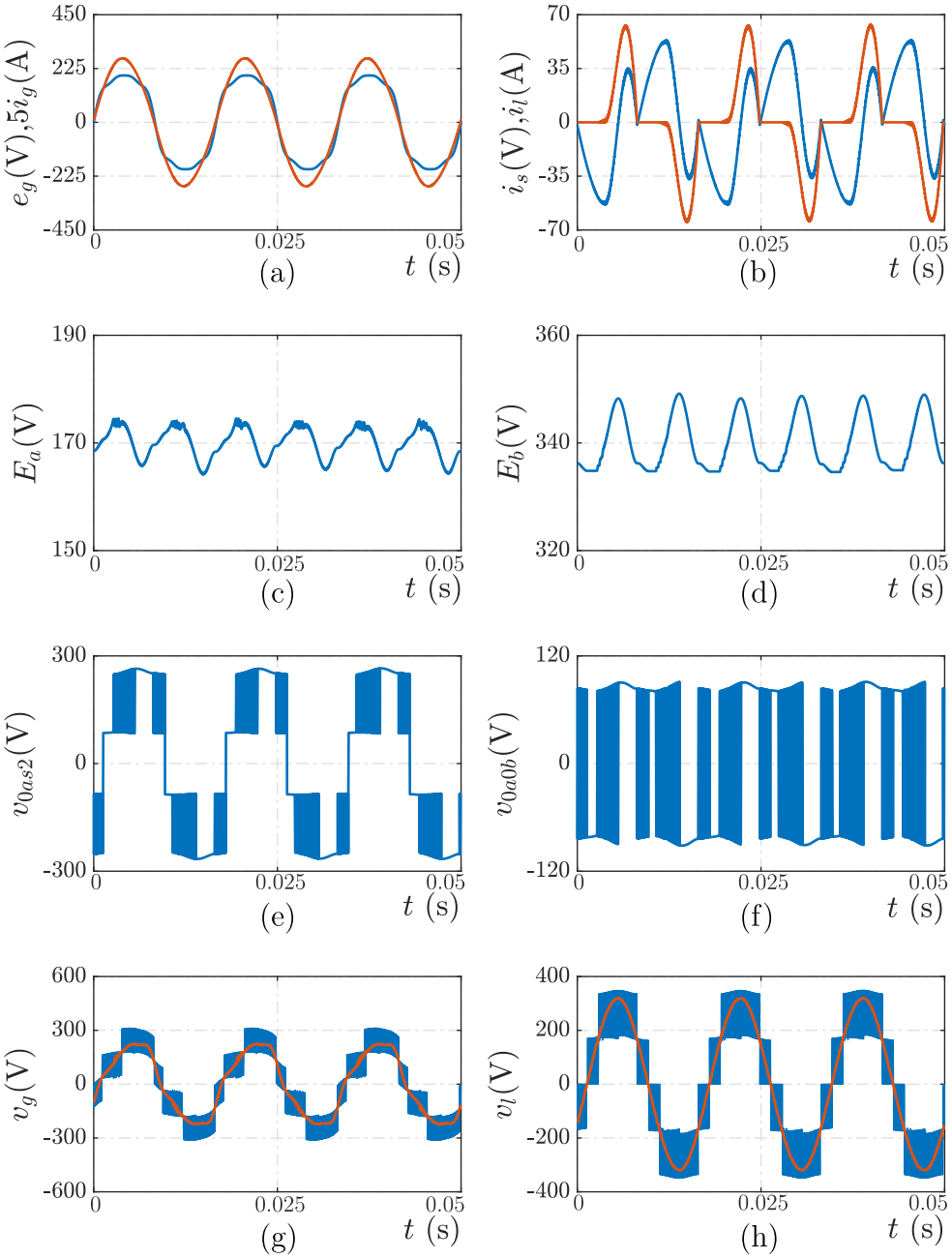


Figure 3.10 – Simulation results of the proposed converter operating with grid voltage and load current disturbances under 30% of grid voltage swell. (a) Grid voltage (with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic) and grid current. (b) Load current and shunt compensation current. (c) Dc-link voltages E_a. (d) Dc-link voltages E_b. (e) Packed u-cell (PUC) voltage (v_0s2). (f) Pole voltage v_{0a0b}.(g) Shunt converter voltage. (g) Series converter voltage.

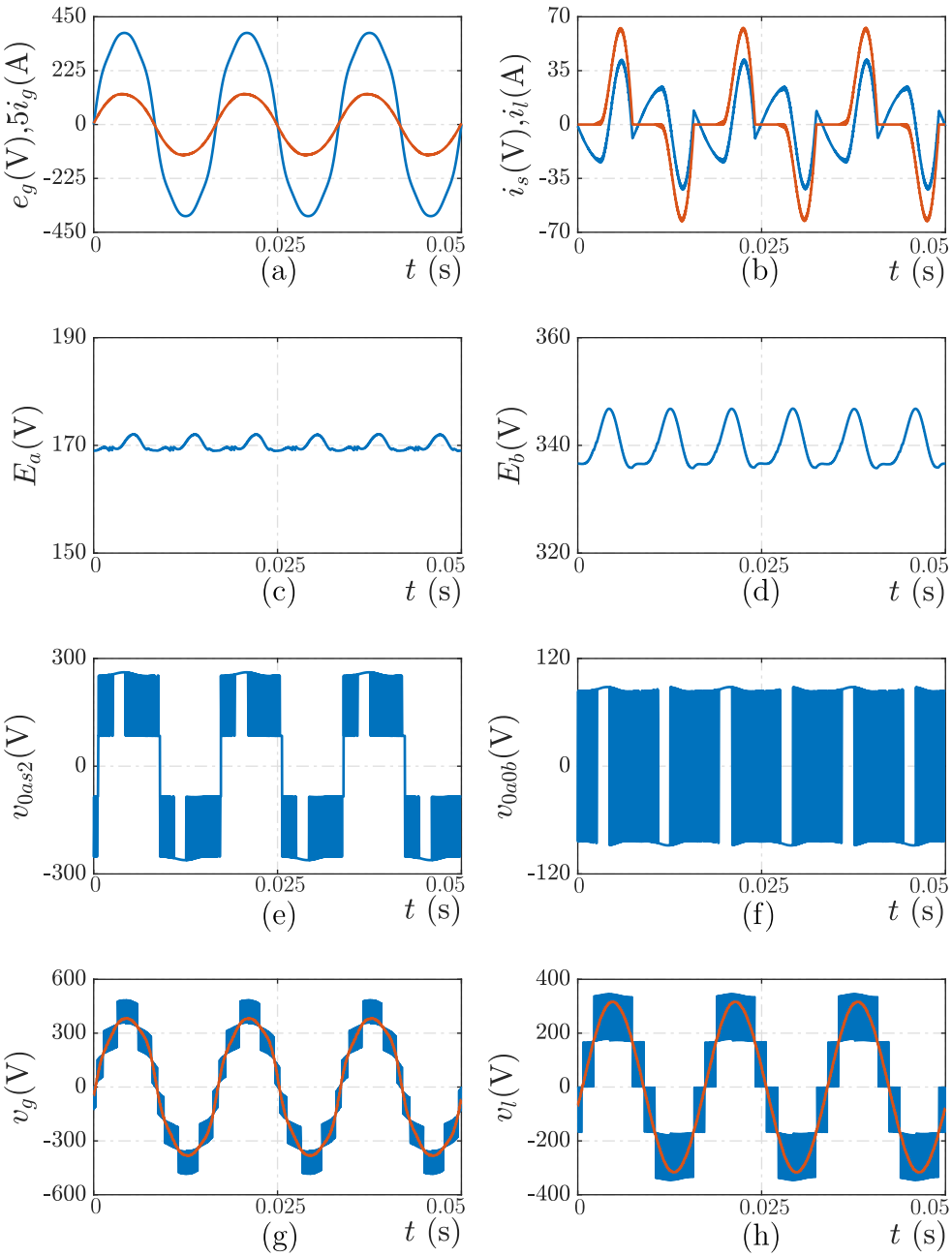


Figure 3.11 – Simulation results of the proposed converter under a voltage sag of 20%.

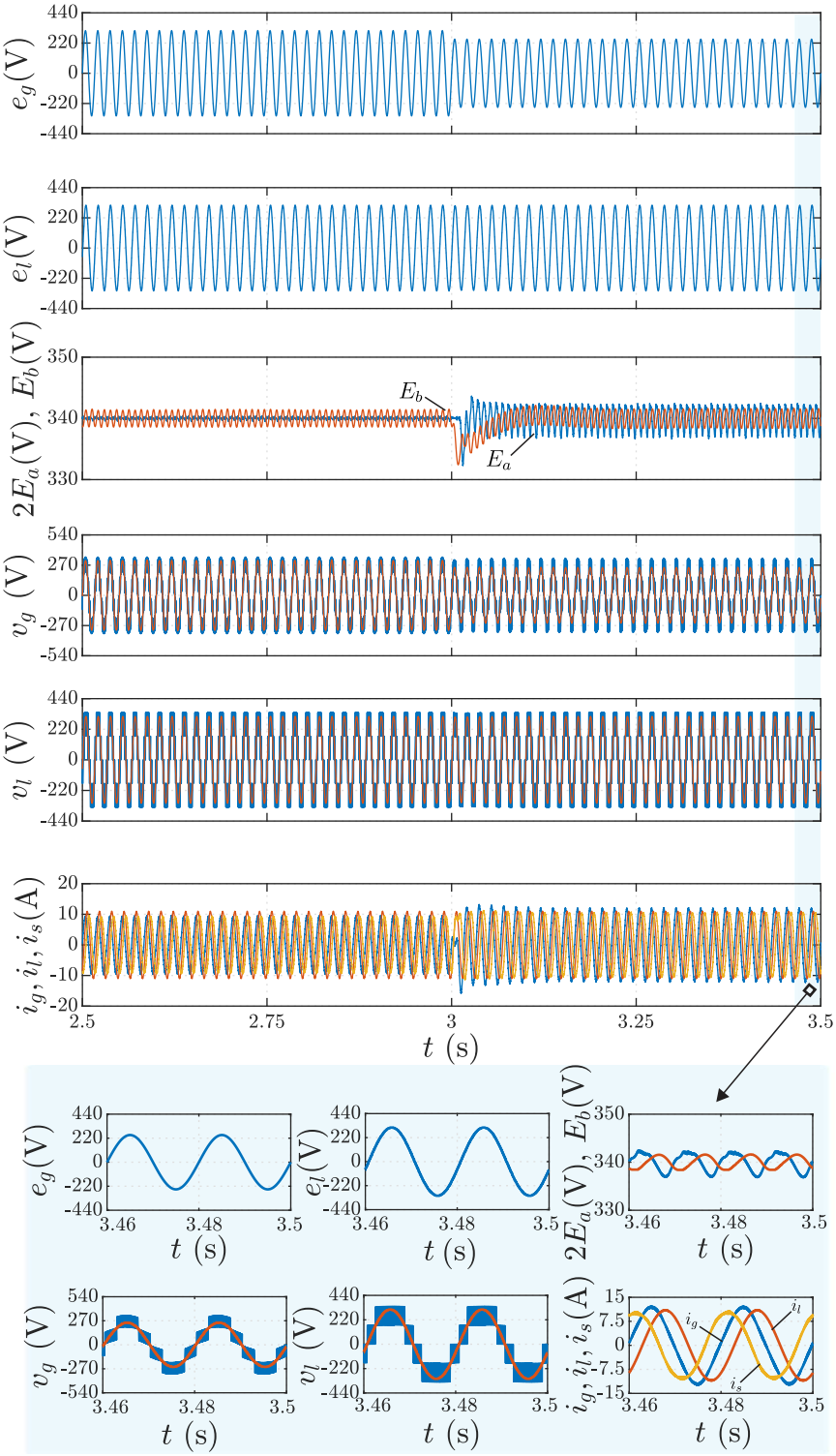


Figure 3.12 – Simulation results of the proposed converter under a voltage swell of 20%.

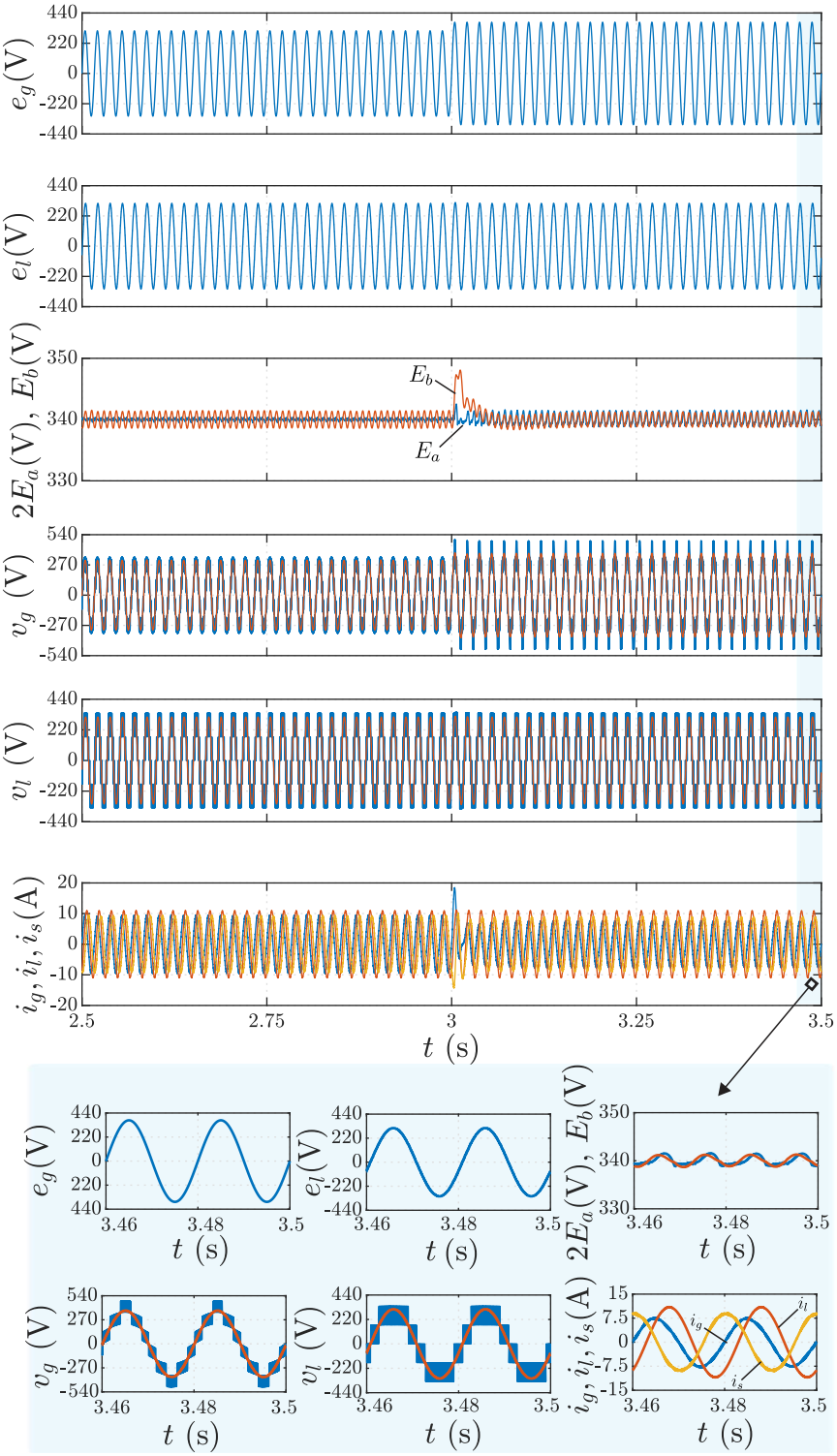
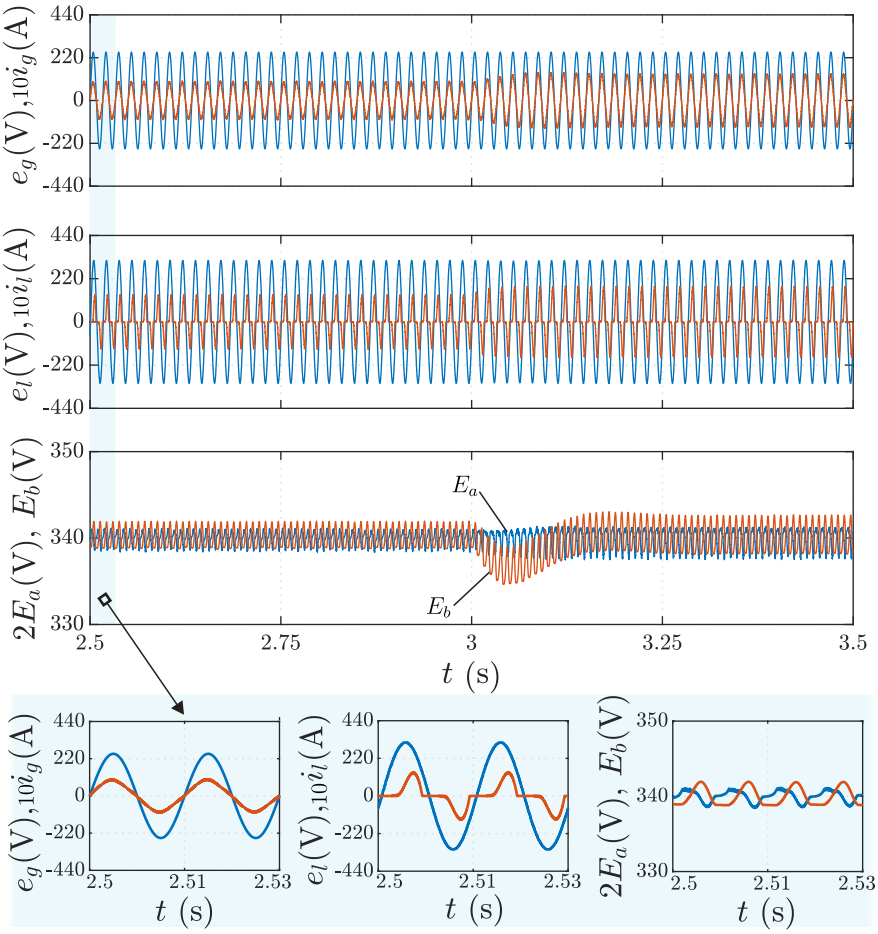


Figure 3.13 – Simulation results of the proposed converter under a 20% of voltage sag and with a step in the load power from $P_l = 1.11$ kW to $P_l = 1.56$ kW.

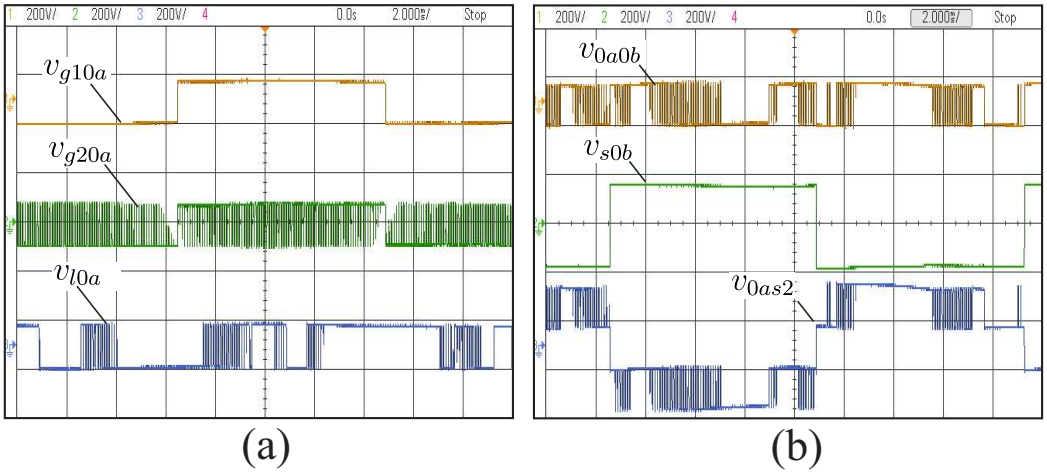


3.5.2 Experimental Results

Experimental results for the proposed 4L-PUC converter were made to validate the simulation tests. First, the pole voltage of each leg is shown in Fig 3.15. Also, the waveforms of the voltage between the dc-links midpoints (v_{0a0b}) and the voltage between the dc-link midpoint of C_a and leg $s2$ (v_{0as2}) are shown. It can be seen that the voltage v_{0a0b} generates two levels [-$(E_b - E_a)/2$, $(E_b - E_a)/2$] and the voltage v_{s0b} generates four levels [(-$E_b + E_a/2$), -$E_a/2$, $E_a/2$, $(E_b - E_a/2)$]. Additionally, notice that the legs $g1$ and $s2$ operate at the line frequency.

The experimental efficiency for both studied configurations was evaluated and are depicted in Fig. 3.15. The results were performed considering the parameters presented in Table 3.4. Notice that these parameters are similar to those used in Table 3.6 to estimate semiconductor losses using the thermal modules. The three cases investigated in section V were also considered here: (a) rated conditions, (b) 20% of grid voltage sag, and (c) 20% of grid voltage swell. The efficiency was calculated for each scenario and is shown in Table 3.5, considering the measured voltages (e_g, e_l) and currents (i_g, i_l). As expected, the

Figure 3.14 – Experimental results of the pole voltage of each leg, the voltage between the dc-links midpoints (v_{0a0b}), and the voltage between the dc-link midpoint of C_a and leg $s2$ (v_{0as2}).



proposed structure has higher efficiency than the conventional one. Moreover, observing Table 3.9, one noticed a similar tendency between the simulation and experimental values obtained for each scenario of the grid voltage.

Table 3.5 – Experimental efficiency values for 4L-PUC and 4L.

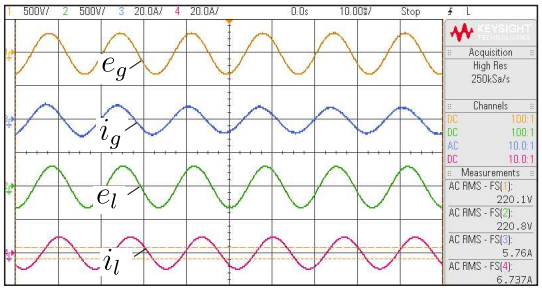
Converter	$E_f(\%)$		
	Case 1	Case 2	Case 3
4L	89.84	88.22	92.90
4L-PUC	92.45	91.86	93.37

Fig. 3.16 shows experimental tests considering the operation in rated conditions and under grid voltage disturbances. In this case, a single-phase rectifier was used as a nonlinear load. From top to bottom, Fig. 3.16(a) depicts the grid voltage (e_g) and current (i_g), as well as the series converter voltage (v_l) and the load current (i_l) in rated conditions. Still in nominal conditions, from top to bottom, Fig. 3.16(b) presents the series (v_l) and shunt (v_g) converter voltages and the grid and load currents. Fig. 3.16(c) and 3.16(d) show the same variables that those presented in Fig. 3.16(b), but operating under 20% of voltage sag and 20% of voltage swell, respectively.

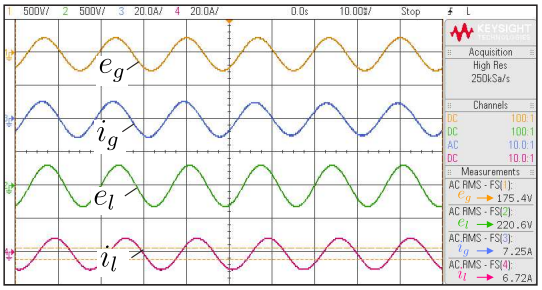
Fig. 3.17 and 3.18 bring results for 4L-PUC converter feeding an RL load. These results demonstrated the operation during 20% of grid voltage sag and swell, respectively. As can be seen, after the disturbance the load voltage maintains its nominal value. Lastly, Fig. 3.19 presents the system behavior already operating with 27% of grid voltage swell, and at a certain instant, a step in the load power from $P_l = 550$ W to $P_l = 850$ W was applied. In this test, the 4L-PUC feeds the aforementioned nonlinear load. Notice that the shunt and series compensation current is guaranteed before and after the load power transient.

Figure 3.15 – Experimental results of the pole voltage of each leg, the voltage between the dc-links midpoints (v_{0a0b}), and the voltage between the dc-link midpoint of C_a and leg $s2$ (v_{0as2}).

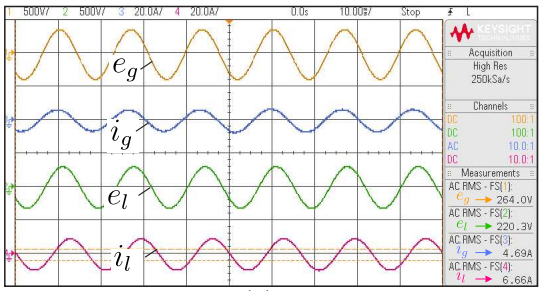
4L-PUC



(a)

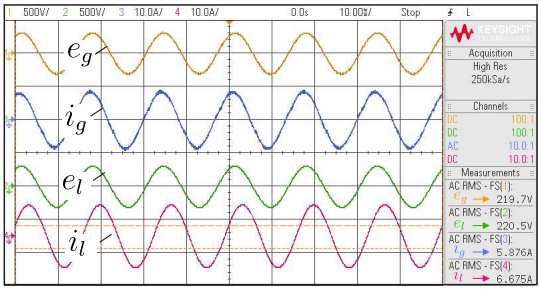


(b)

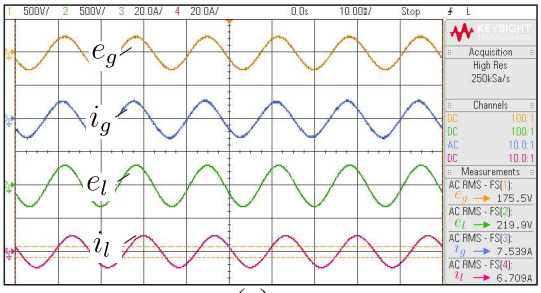


(c)

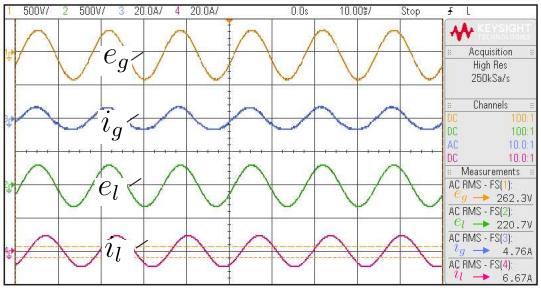
4L



(d)

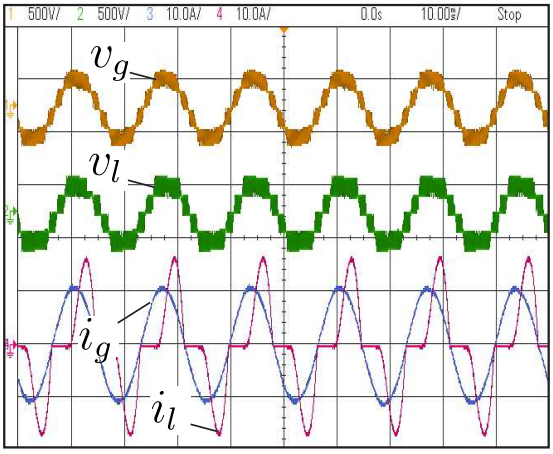


(e)

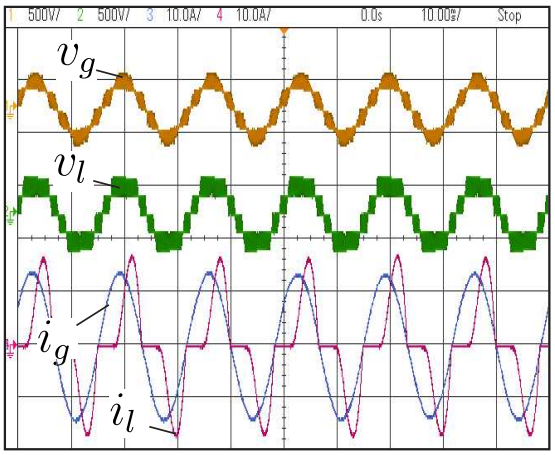


(f)

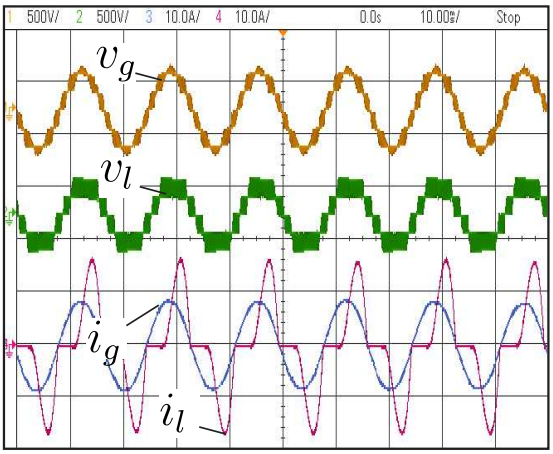
Figure 3.16 – Experimental results. Series converter voltage (v_l), shunt converter voltage (v_g), grid current (i_g), and load current (i_l) (a) in rated condition; (b) under 20% of voltage sag; (c) uder 20% of voltage swell.



(a)

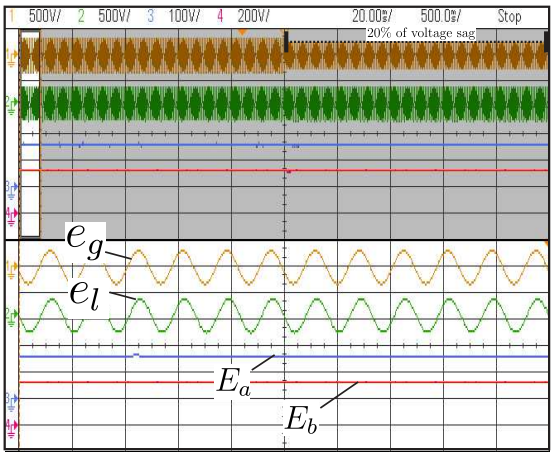


(b)

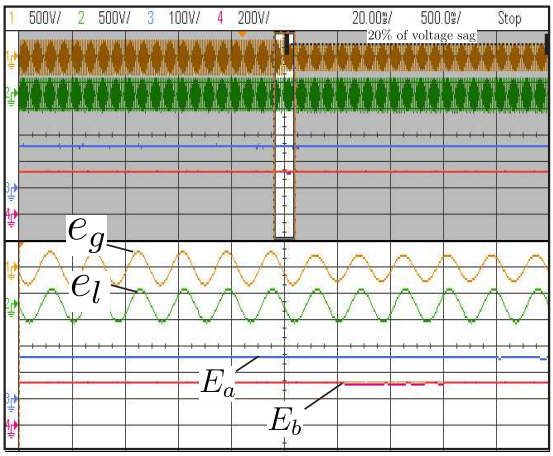


(c)

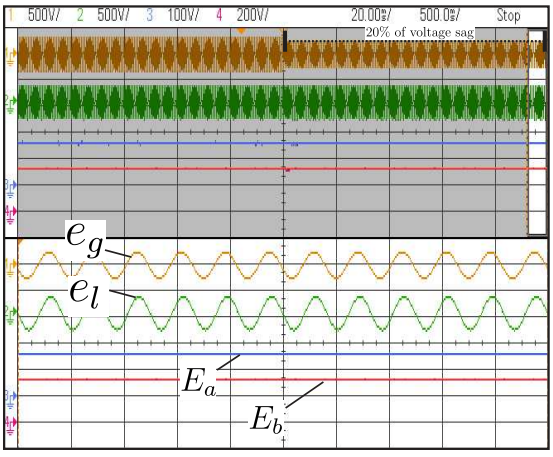
Figure 3.17 – Experimental results - Grid voltage sag of 20%. Grid (e_g) and load voltages (e_l) and dc-link voltages (E_a and E_b) (a) in rated conditions (b) in the beginning of the disturbance, and (c) under 20% of voltage sag.



(a)

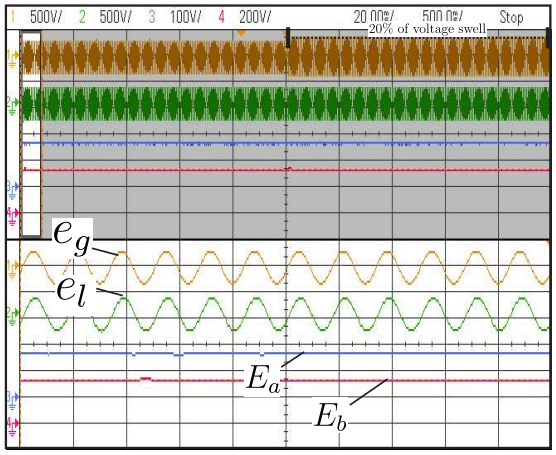


(b)

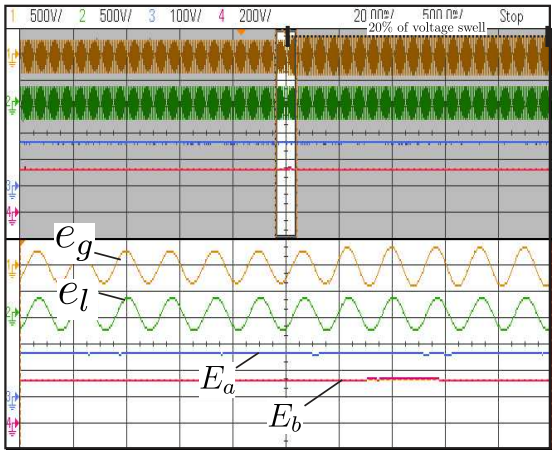


(c)

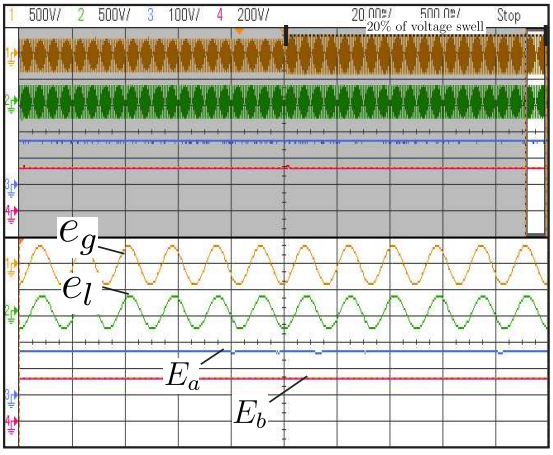
Figure 3.18 – Experimental results - Grid voltage swell of 20%. Grid (e_g) and load voltages (e_l) and dc-link voltages (E_a and E_b) (a) in rated conditions (b) in the beginning of the disturbance, and (c) under 20% of voltage swell.



(a)

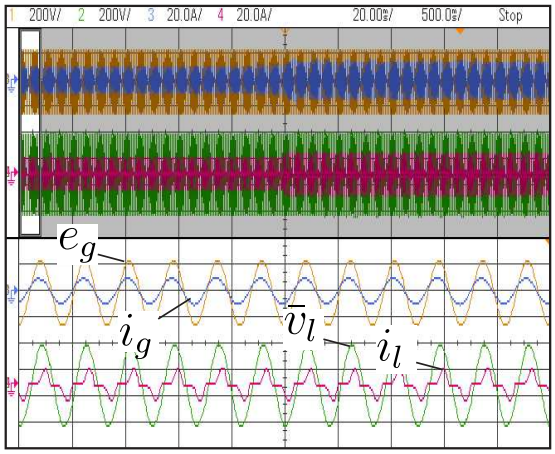


(b)

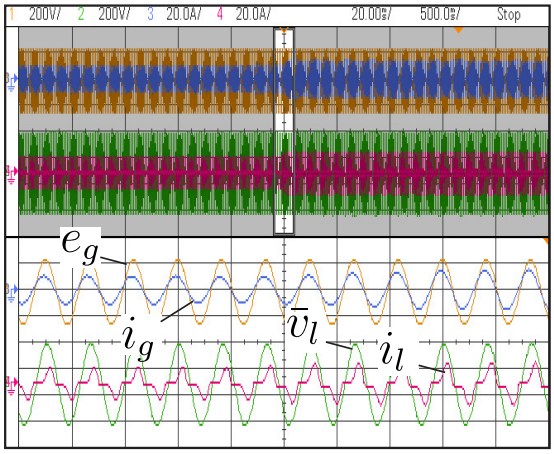


(c)

Figure 3.19 – Experimental results - Step in the load power from $P_l = 1.11$ kW to $P_l = 1.56$ kW and grid voltage under 20% of voltage sag. (a) Average series converter voltage ($\bar{v}_l$), grid voltage (e_g), grid current (i_g), and load current (i_l) (a) before the load transient, (b) in the beginning of the load transient, and (c) during the load transient.



(a)



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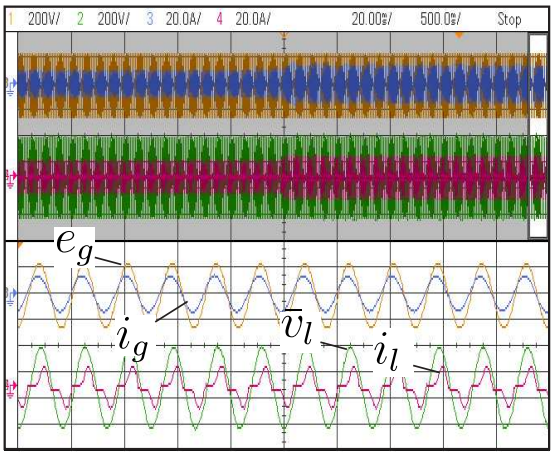


(c)

3.6 Comparison of the Topologies

In this section, 4L and 4L-PUC converters are analyzed in terms of transformer rating, voltage stress on the power switches, average switching frequency, harmonic distortion, ac-filter size, and power losses. The simulation has been performed in closed-loop control and the specifications presented in Table 3.6 were considered. The analysis related to the average switching frequency, harmonic distortion, and power losses takes into account the three cases:

- Case 1 - Rated condition;
- Case 2 - 20% of grid voltage sag;
- Case 3 - 20% of grid voltage swell.

Figure 3.20 – Conventional single-phase ac-dc-ac 4L converter.

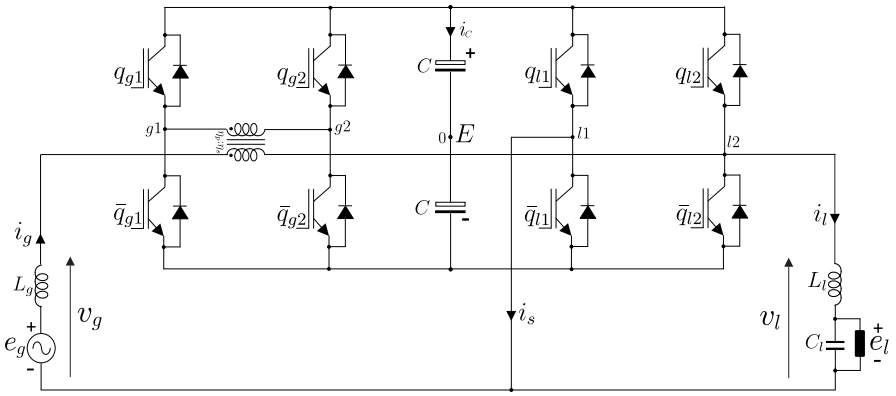


Table 3.6 – Parameters considered for the tests.

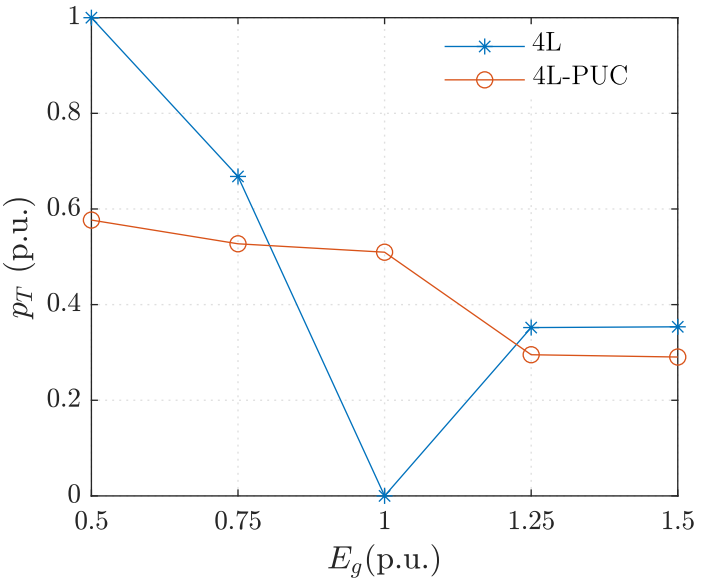
Parameter		Value
Rated load power	P_l	1 kW
Load power factor	$\cos(\delta_l)$	0.8
Series reference voltage amplitude	V_l^*	311 V
Grid voltage amplitude	E_g^*	311 V
Dc-link voltage - 4L-PUC	E_a, E_b	340/170 V
Dc-link voltage - 4L	E	340 V
Transformer turn ratio - 4L-PUC	η	1
Transformer turn ratio - 4L	η	2
Switching frequency	f_s	10 kHz
Grid and load frequency	f_g/f_l	60/60 Hz
Grid inductance	L_g	5 mH
Grid resistance	R_g	0.2 Ω

3.6.1 Transformer Rating

The design of the transformer has a dominant impact on the overall system's cost-effectiveness. Depending upon the application, the weight and volume are important goals to minimization, especially in line-frequency transformers. In this way, the power processed by the transformer can be considered a constraint that can be observed for optimization. Fig. 3.21 presents the apparent power on the transformer of the conventional and proposed converter considering a variation in the amplitude of the grid voltage from $E_g = 0.5$ to 1.5 p.u.

Since the transformer of the 4L converter can be disabled in rated conditions, it does not process power. Otherwise, under voltage transients, the transformer power is directly proportional to the magnitude of the disturbance. The worst case for the 4L converter is when it has to deal with voltage sags, processing values close to the rated power when $E_g = 0.5$ pu. In this scenario, the apparent power on the transformer of the proposed configuration is 42% lower than the conventional one.

Figure 3.21 – Power processed by the transformer as a function of the amplitude of the grid voltage.



3.6.2 Rating of the Semiconductor Devices

Table 3.7 summarizes the voltage and frequency ratings of the power switches of the 4L and 4L-PUC converters. In both configurations, the voltage stresses are normalized considering the total dc-link voltage value needed to obtain $V_l = 311$ V. The average switching frequency of each switch is verified for the three aforementioned cases considering conventional and proposed converters operating with the switching frequency $f_s = 10$ kHz.

The voltage rating of the power switches is defined by the dc-link voltage. For the 4L converter, all switches are submitted to the total dc-link voltage. Whereas, despite having two dc links, in the proposed converter, the devices, except for leg $s2$, have half of the reverse voltage when compared to the 4L converter.

Observing Table 3.7, in the three cases, the switches of legs $g1$ ($q_{g1} - \bar{q}_{g2}$) and $s2$ ($q_{s2} - \bar{q}_{s2}$) operate in the line frequency. Besides that, analyzing the overall average switching frequency for both studied configurations [4L-PUC - $f_{m_{ov}}$=$(f_{qg1} + f_{qg2} + f_{ql} + f_{qs1} + f_{qs2})/5$; 4L-$f_{m_{ov}}$=$(f_{qg1} + f_{qg2} + f_{ql1} + f_{ql2})/4$], the proposed one presents a reduction of 36%, 45%, and 66% for the cases 1, 2, and 3, respectively, when compared to conventional 4L converter. As can be seen, although the switches of leg $s2$ have a voltage blocking of 1.09 p.u., they switch in the line frequency. The other legs of the structure have half of the voltage blocking compared to leg $s2$, however, legs $g2$ and l operate with a higher switching frequency. This attribute allows a better distribution of the switching losses between the power switches of the proposed configuration, contributing to the reduction of its total switching losses. Also, can be noticed a tendency of the proposed converter to present better efficiency compared to the conventional 4L configuration, even though it has two more power switches.

Table 3.7 – Rating of the semiconductor devices.

4L					
Leg	q_{g1}	q_{g2}	q_{l1}	q_{l2}	
Voltage (p.u.)	1.09	1.09	1.09	1.09	
f_s(kHz) - Case 1	10.17	9.9	9.9	0.45	
f_s(kHz) - Case 2	10.17	9.60	9.60	0.75	
f_s(kHz) - Case 3	5.88	10.02	5.82	4.71	
4L-PUC					
Leg	q_{g1}	q_{g2}	q_l	q_{s1}	q_{s2}
Voltage (p.u.)	0.54	0.54	0.54	0.54	1.09
f_s(kHz) - Case 1	0.06	9.99	6.4	7.5	0.06
f_s(kHz) - Case 2	0.06	9.99	4.27	6.15	0.06
f_s(kHz) - Case 3	0.06	9.99	5.31	6.43	0.06

3.6.3 Harmonic Distortion

The total harmonic distortion (THD) of the grid and load currents (i_g and l_l) and the weighted total harmonic distortion (WTHD) of the shunt and series converter voltages (v_g and v_l) have been calculated in percentage form to compare the studied topologies. According to (HOLMES; LIPO, 2003), the THD and WTHD can be calculated, respectively, by

$$THD(\%) = \frac{100}{\gamma_1}\sqrt{\sum_{n=2}^{N_h}\gamma_n^2}, \tag{3.27}$$

$$WTHD(\%) = \frac{100}{\gamma_1}\sqrt{\sum_{n=2}^{N_h}\left(\frac{\gamma_n}{n}\right)^2}, \tag{3.28}$$

where γ_1 is the amplitude of the fundamental component, γ_n is the amplitude of the harmonic of order n, and N_h is the number of harmonics that are used in the calculation. Both THD and WTHD were obtained using $Nh = 100$ components.

Fig. 3.22 shows the shunt and series converter voltage of the 4L converter considering the three cases of operation. Notice that, the studied conventional converter can generate the voltage v_g with up to not equally spaced seven levels when dealing with swells and v_l with at best three levels in any case. Observing Fig. 3.23, it can be seen that the proposed configuration can generate the voltage v_g with up to equally spaced seven levels under swells and v_l with five levels for any case.

Table VI details the THD and WTHD for the studied configurations. Taking into account the design of the ac filters (L_g, L_l, C_l), the worst scenario may be considered. Observing Table VI, this occurs during the grid voltage swell. In this case, the proposed converter can reduce the THD of i_g and i_l up to 24% and 47%, respectively, when compared with the 4L converter. These improvements make it possible to reduce the ac-filter size, especially on the load side, as will be shown in the following section.

Figure 3.22 – Voltages generated by the 4L converter and their average values ($\bar{v}_g$ and $\bar{v}_l$). (a) Shunt converter voltage in rated conditions. (b) Shunt converter voltage under 20% of voltage sag. (c) Shunt converter voltage under 20% of voltage swell. (d) Series converter voltage for any operation scenario.

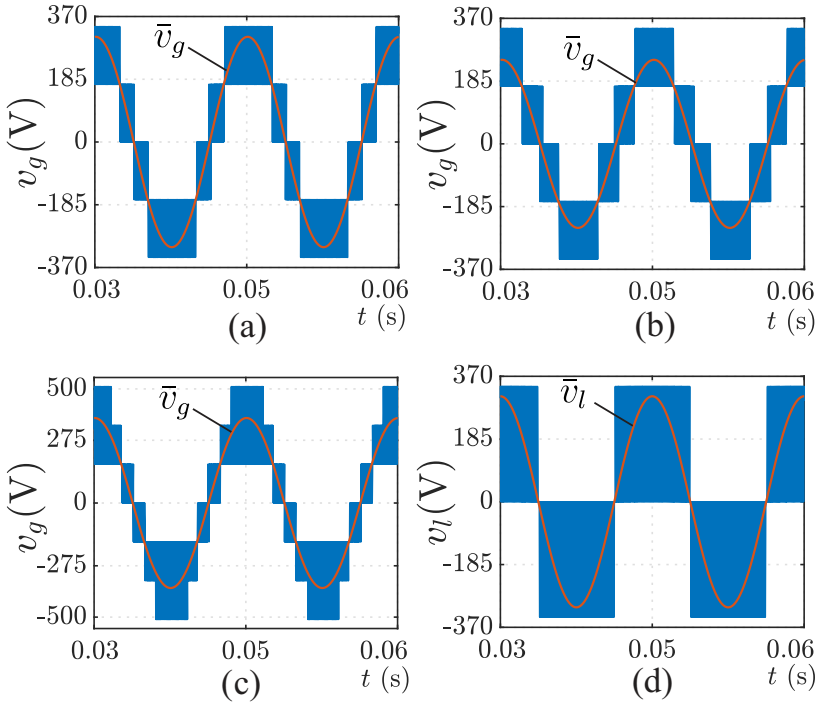


Figure 3.23 – Voltages generated by the 4L-PUC converter and their average values ($\bar{v}_g$ and $\bar{v}_l$). (a) Shunt converter voltage in rated conditions. (b) Shunt converter voltage under 20% of voltage sag. (c) Shunt converter voltage under 20% of voltage swell. (d) Series converter voltage for any operation scenario.

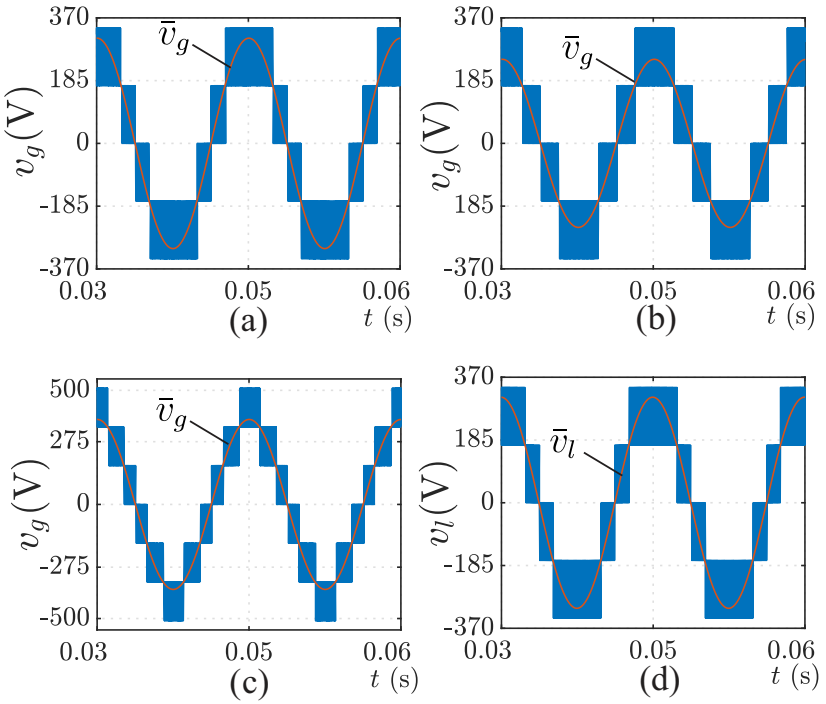


Table 3.8 – Voltage WTHD and current THD analysis.

Case 1				
Converter	THD (%)		WTHD (%)	
	i_g	i_l	v_g	v_l
4L	3.76	0.51	0.16	0.31
4L-PUC	3.60	0.27	0.14	0.16
Case 2				
Converter	THD (%)		WTHD (%)	
	i_g	i_l	v_g	v_l
4L	3.92	0.51	0.23	0.31
4L-PUC	2.71	0.27	0.15	0.16
Case 3				
Converter	THD (%)		WTHD (%)	
	i_g	i_l	v_g	v_l
4L	4.33	0.51	0.13	0.31
4L-PUC	3.25	0.27	0.09	0.16

3.6.4 AC-Filter Design

This section presents the design of the minimum filter inductance L_k ($k = g, l$) using the criterion of the maximum current ripple Δi_k (LANGE et al., 2015). This study takes

into account the voltage across the ac-filters as well as the variation of the instantaneous phase angle of the grid or load voltage ($\theta_k = 2\pi f_k t$) and modulation index (m_k). Since the converter synthesizes five levels in the series and shunt converter voltages during rated and voltage sags scenarios, i.e., in the worst cases, the behavior of Δi_k should be analyzed for m_k lower and higher than 0.5. In this way, as the average voltage across the inductor is zero during a switching period and its instantaneous voltage can be defined as $v_{Lk} = L_k \frac{\Delta i_k}{\Delta t}$, the following equation can be defined

$$\frac{L_k \Delta i_k}{E_r T_s} = \begin{cases} m_k \sin(\theta_k) - 2m_k^2 \sin^2(\theta_k), \ m_k < 0.5 \\ 3m_k \sin(\theta_k) - 2m_k^2 \sin(\theta_k)^2 - 1, \ m_k \geq 0.5 \end{cases}, \tag{3.29}$$

where $0 \leq \theta_k \leq \pi$, $E_r = E_b = 2E_a$ and the term $\frac{L_k \Delta i_k}{E T_s}$ is defined as a normalized current ripple, called here $\overline{\Delta} i_k(m_k, \theta_k)$. Hence, the minimum inductance value can be obtained considering the maximum normalized current ripple value, which yields

$$L_{k_{\min}} = \frac{E_r}{f_s \Delta i_k} \max[\overline{\Delta i_k}(m_k, \theta_k)]. \tag{3.30}$$

The profile of the normalized current ripple was verified considering a variation in the grid or load instantaneous phase angle from $\theta_k = 0$ to π and for some modulation index values higher than 0.5. It was verified that, for any scenario, the maximum normalized current ripple value is equal to 1/8. Therefore, the minimum inductance value of the proposed converter can be computed as follows

$$L_{k_{\min}} = \frac{E_r}{8 \Delta i_k f_s}. \tag{3.31}$$

Considering this same methodology to calculate the L_k values for the 4L converter, since it presents five levels at the shunt side, the $L_{g_{\min}}$ value is similar for both converters. On the other hand, as the conventional one generates three levels at the series side, the maximum normalized current ripple value is equal to 1/4, which allows a reduction of $L_{l_{\min}}$ in 50% for the 4L-PUC converter, considering the same current ripple. More details about the inductor filter design can be found in Appendix A.

When determining $L_{\min}$, the output filter capacitance (C_l) can be calculated from the resonant frequency (f_r) expression considering the following condition: $10 f_l < f_r < f_s/10$ (LI et al., 2014).

3.6.5 Power Losses Analysis

Semiconductor power losses were performed using thermal modules. The power switches chosen were IGBT SKM50GB063D from Semikron. The power losses calculation includes the conduction (P_{cd}), switching (P_{sw}), and total power losses ($P_t = P_{cd} + P_{sw}$).

Table 3.9 presents the conduction, switching, and total power losses values for the three cases of operation (rated, sag, and swell). It was considered a rated power of 1 kW, and the switching frequency was established in $f_s = 10$ kHz. As can be seen, the proposed converter presents higher conduction losses, since it had more power switches in the current path compared to the conventional configuration. Nevertheless, its reduced switching losses are justified by the switching frequency of the devices, associated with the maximum voltage across the switch during the off state (see Table 3.7). The decrease in switching losses on the 4L-PUC converter compensates the increasing in the conduction losses. Therefore, it can be seen that the proposed topology had lower total power losses than the conventional one. Notice that, the proposed configuration is suitable for applications with high voltages and low currents. Furthermore, these results can be improved for the 4L-PUC converter by selecting the THD or WTHD as a standard performance required to make a loss comparison. In this scenario, the switching frequency in the 4L converter needs to be adjusted to meet this requirement, increasing its switching losses.

Table 3.9 – Semiconductor power losses.

Case 1			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
4L	6.30	23.57	29.87
4L-PUC	12.65	4.86	17.52
Case 2			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
4L	7.54	24.16	31.71
4L-PUC	15.07	5.76	20.84
Case 3			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
4L	5.81	19.00	24.81
4L-PUC	11.71	4.54	16.25

3.7 Conclusion

In this Chapter, it was proposed a single-phase ac-dc-ac topology based on packed u-cell for UPQC applications. The configuration is constituted by a four-leg module with a u-cell connected to the common part of the system, which allows generating multilevel waveforms on the grid and load side. The comparative analysis indicated that the proposed converter has lower harmonic distortion, since can reduce the grid and load currents THD up to 24% and 47%, respectively, when compared to 4L. Consequently, this improvement impacted the ac-filter design, in which the proposed converter demonstrated a reduction of 50% in the output filter size compared to 4L converter. Furthermore, at least one leg

of the 4L-PUC can operate at low frequency, reducing switching losses. In this context, the comparative power losses analysis demonstrated that 4L-PUC is more efficient than 4L in high voltage low current applications. The simulation and experimental results demonstrated that the proposed system ensures grid power factor compensation, dc-link voltage regulation, and grid voltage sag and swell mitigation.

Chapter 4

New Decoupling Methods to Improve the Performance of Single-Phase Transformerless Unified Power Quality Conditioners Based on Three-Leg and Five-Leg Converters

4.1 Introduction

In single-phase UPQC applications, three-leg converters (LU et al., 2016; CARDOSO; JACOBINA; FELINTO, 2022) became more suitable than four-leg converters since the number of power switches is minimized, and the line-frequency transformer can be removed without causing circulating current. In addition, the three-leg converter has received more attention in the literature because it presents all switches with half of the reverse voltage compared to a half-bridge configuration (CHEUNG et al., 2017; ABDALAAL; HO, 2022) for the same load voltage amplitude. On the other hand, if the structure is designed to provide voltage swell compensation on the grid side, issues related to the operation with a high dc-link voltage value even under rated conditions are presented. Therefore, this chapter proposes new decoupling methods to improve the performance of single-phase transformerless unified power quality conditioners (UPQC) based on three- and five-leg converters under grid voltage swells. First, a reconfiguration of the three-leg module using a bidirectional switch is proposed to improve the voltage swell capability. Then, two five-leg configurations are presented, one based on three-leg and shunt modules and another based on three-leg and standby converters. The systems

studied provide a unity power factor on the grid side with high power quality and feed the load with a sinusoidal waveform during both voltage swell and sag. The system model, dc-link voltage specifications, pulse-width modulation (PWM) techniques, and overall control strategies are presented. Simulation and experimental results are also addressed to evaluate the feasibility of the proposed systems.

4.2 Three-Leg Converter (3LS-UPQC)

In this section, a new method for decoupling the series and shunt converters for the three-leg ac-dc-ac is proposed. This method makes it possible to decouple the operation under nominal conditions and grid voltage sags of the transients of the grid voltage swells. The topology is composed of three two-level legs such that the leg directly connected to the grid positive terminal is shared by shunt and series converters. The system provides a unity power factor at the grid side with high power quality and feeds the load with a sinusoidal waveform in both voltage swell and sag events. System model, dc-link voltage specifications, PWM techniques, and overall control strategies are presented. Additionally, simulation and experimental results are addressed to evaluate the feasibility of the proposed system.

4.2.1 System Model

Figure 4.1 – Proposed 3LS-UPQC configuration.

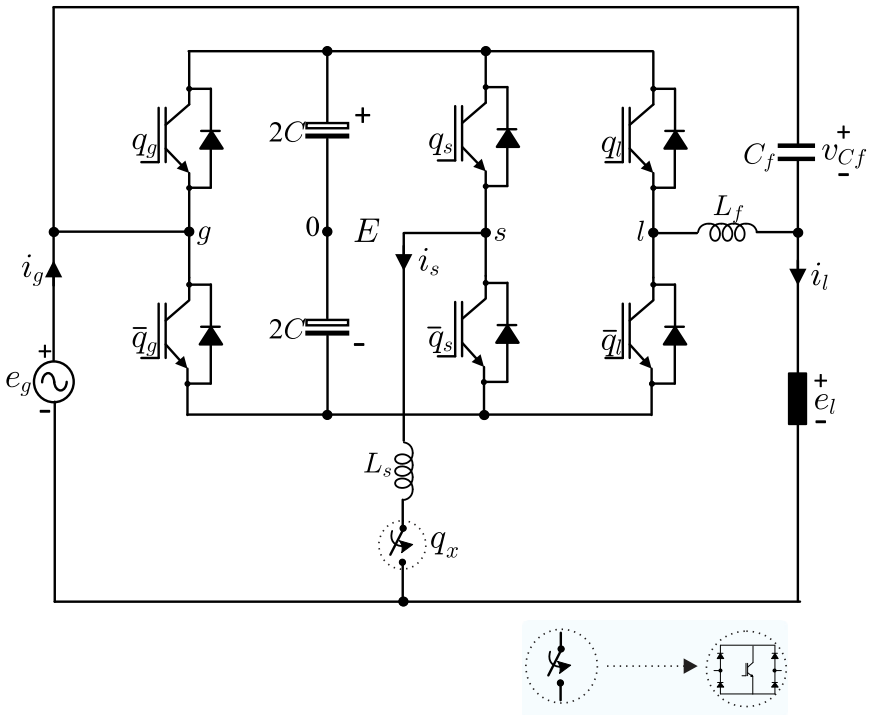


Figure 4.2 – Equivalent circuit.

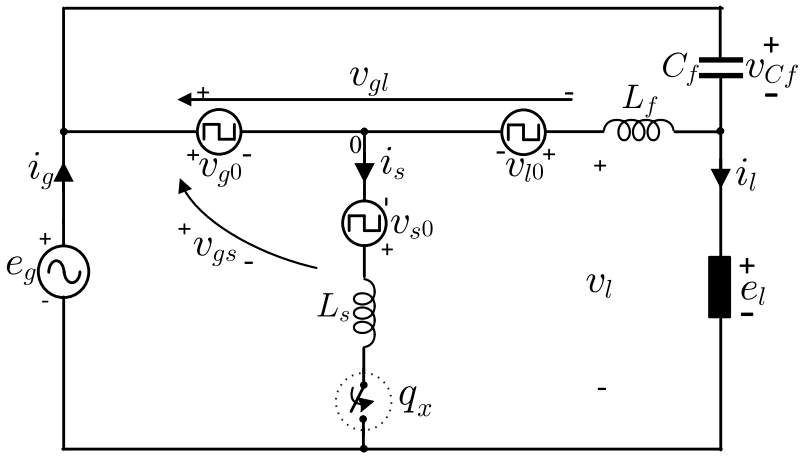


Fig. 4.1 presents the proposed single-phase three-leg UPQC (3LS-UPQC). Such a configuration is constituted by a single-phase grid and load voltages (e_g and e_l), three two-level legs, inductor and capacitor filters (L_s, C_f, and L_f), one dc link capacitor bank (C), and a bidirectional switch (q_x) in series with the leg s. The controlled legs are composed by top switches q_g, q_l, and q_s and complementary bottom switches $\bar{q}_g$, $\bar{q}_l$, and $\bar{q}_s$. In this structure, the leg constituted by the switches q_g–$\bar{q}_g$ is shared between the shunt and series converters.

Fig. 4.2 presents the simplified equivalent circuit of the proposed configuration, where v_{gs}, v_{gl}, v_{Cf}, and v_l are the shunt converter voltage, series converter voltage, output filter voltage, and converter output voltage, respectively; i_g, i_l, and i_s are the grid current, load current, and shunt compensation current, respectively. From Kirchhoff's voltage law and considering that q_x is closed, the shunt converter voltage (v_{gs}), series converter voltage (v_{gl}), output filter voltage (v_{Cf}), and converter output voltage are defined (v_l), respectively, as

$$v_{gs} = v_{g0} - v_{s0}, \tag{4.1}$$

$$v_{gl} = v_{g0} - v_{l0}, \tag{4.2}$$

$$v_{Cf} = e_g - e_l, \tag{4.3}$$

$$v_l = e_g - v_{gl}, \tag{4.4}$$

where v_{g0}, v_{l0}, and v_{s0} are the pole voltages of the converter, which can be denoted as v_{j0} = $(2q_j$ - $1)E/2$, with $j = g, l, s$. E is the dc-link voltage. Assuming that the switch q_x is opened, from Kirchhoff's voltage law, the load voltage can be defined by (4.3) or (4.4).

4.2.2 Dc-link Voltage Specifications

Hereafter, the symbol * is used to reference variables. The reference voltages v_{gs}^* and v_{gl}^* can only be correctly synthesized if the reference dc-link voltage of the proposed 3LS-UPQC obey the following condition

$$E^* \geq \max\{|v_{gs}^*|, |v_{gl}^*|, |v_{gs}^* - v_{gl}^*|\}. \tag{4.5}$$

Defining

$$v_{gs}^* = V_{gs}^* \sin(\omega t + \gamma_g), \tag{4.6}$$

and

$$v_{gl}^* = V_{gl}^* \sin(\omega t + \gamma_g + \epsilon) = E_g \sin(\omega t) - V_l^* \sin(\omega t + \gamma_l), \tag{4.7}$$

thus, from trigonometric analysis and taking into account equation (4.5), one can define

$$|v_{gs}^*| \leq E^*, \tag{4.8}$$

$$|v_{gl}^*| \leq E^*, \tag{4.9}$$

$$|v_{gs}^* - v_{gl}^*| \leq E^*. \tag{4.10}$$

As described by equation (4.10), the dc-link voltage required for the three-leg converter depends on the amplitude of both the series and shunt converter voltages. On the series side, the voltage needed to generate correctly the load voltage considers the range of the grid voltage sag or swell that the converter is designed to support. For example, if the converter is designed to deal with up to 1 p.u. of sags and swells, the dc-link voltage must has at least 1 p.u. available. The shunt unit needs a sufficient voltage to ensure proper grid current generation, which is defined by

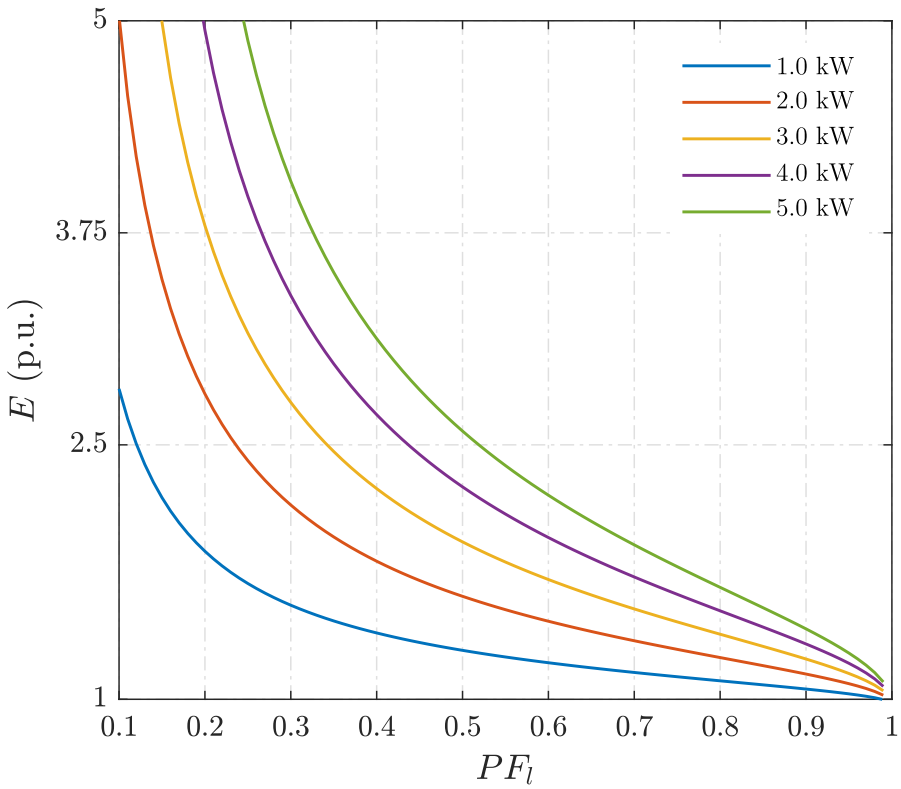
$$V_{gs} = E_g - I_s(R_s + jX_s). \tag{4.11}$$

Combining with (4.8), one can define the following relationship that must be respected:

$$E \geq |E_g - I_s(R_s + jX_s)|, \tag{4.12}$$

where R_s denotes the intrinsic resistance of the inductor L_s, and X_s represents its reactance. From (4.12), one can see that the dc-link voltage of the three-leg converter is influenced not only by the grid voltage value, but also by the shunt compensation current, indicating a dependence on the load characteristics. From (4.11), steady-state simulations were performed to verify the operations constraints of the dc-link voltage (E) of the three-leg converter considering a variation in the load power factor from $PF_l = 0.1$ to 1 and the active power from $P_l = 1$ kW to 5 kW, grid and load voltage amplitude $E_g = E_l = 155.6$ V, and switching frequency $f_s = 10$ kHz. Fig. 4.3 depicts the behavior of the dc-link voltage value for each scenario of active power and load power factor. As can be seen, the dc-link voltage required to generate v_{gs} correctly increases with the decrease in the load power factor.

Figure 4.3 – Operations constraints of the dc-link voltage (E) of the three-leg converters considering a variation in the load power factor and load active power.



4.2.3 PWM Strategy

This section presents the PWM strategies used to control the proposed 3LS-UPQC. In this way, two operation scenarios are considered, one for the operation with voltage

during rated and grid voltage sag condition and the other for the operation with grid voltage swell.

4.2.3.1 Ac-dc-ac Operation

Considering scenarios under rated conditions or with voltage sags, the studied topology has a similar operation when compared to other shared-leg ac-dc-ac topologies. In this context, in the ac-dc-ac operation, a Space-Vector PWM strategy (SVPWM) and a Scalar PWM are developed here.

- **SVPWM Strategy**

Fig. 4.4 presents the space-vector plane generated by the proposed 3LS-UPQC considering $E = 1$ pu. A voltage vector can be generated by a given switching combination and is denoted by $\mathbf{v}_k = v_{gs} + \mathrm{j}v_{gl}$. The voltages v_{gs} and v_{gl} represent the real and imaginary axis, respectively, and the vectors in the plane are represented as $\mathbf{v}_k$, where k is the binary sequence $\{q_g, q_l, q_s\}$. For example, the voltage vector $\mathbf{v}_{100}$ corresponds to $\{q_g = 1, q_l = 0, q_s = 0\}$. The switching conduction state is represented by 1 for a closed switch and 0 for an opened switch.

Since $\mathbf{v}^* = v_{gs}^* + \mathrm{j}v_{gl}^*$ represents the reference voltage vector that must be generated by the converter during the sampling period T, the reference voltage located within a sector ($K = 1, 2, ..., 6$), is synthesized by the three nearest voltage vectors. These vectors are defined as $\mathbf{v}_a$, $\mathbf{v}_b$, and $\mathbf{v}_c$. Considering $\mathbf{v}^*$ constant during a sampling period T, it can be written that

$$\mathbf{v}^* = \frac{t_a}{T}\mathbf{v}_a + \frac{t_b}{T}\mathbf{v}_b + \frac{t_c}{T}\mathbf{v}_c, \tag{4.13}$$

$$T = t_a + t_b + t_c, \tag{4.14}$$

where t_a, t_b, and t_c represents the application times of the vectors v_a, v_b, and v_c, respectively. These time lengths can be determined by (4.15). The shunt and series converter voltages generate for each voltage vector in the space-vector plane, as well as the vector sequence chosen for each sector is described in Table 4.1.

$$\begin{bmatrix} t_a \\ t_b \\ t_c \end{bmatrix} = \begin{bmatrix} \frac{\mathrm{Re}(\mathbf{v}_a)}{T} & \frac{\mathrm{Re}(\mathbf{v}_b)}{T} & \frac{\mathrm{Re}(\mathbf{v}_c)}{T} \\ \frac{\mathrm{Im}(\mathbf{v}_a)}{T} & \frac{\mathrm{Im}(\mathbf{v}_b)}{T} & \frac{\mathrm{Im}(\mathbf{v}_c)}{T} \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} v_{gs}^* \\ v_{gl}^* \\ T \end{bmatrix}. \tag{4.15}$$

Figure 4.4 – Space-vector plane generated by the proposed 3LS-UPQC.

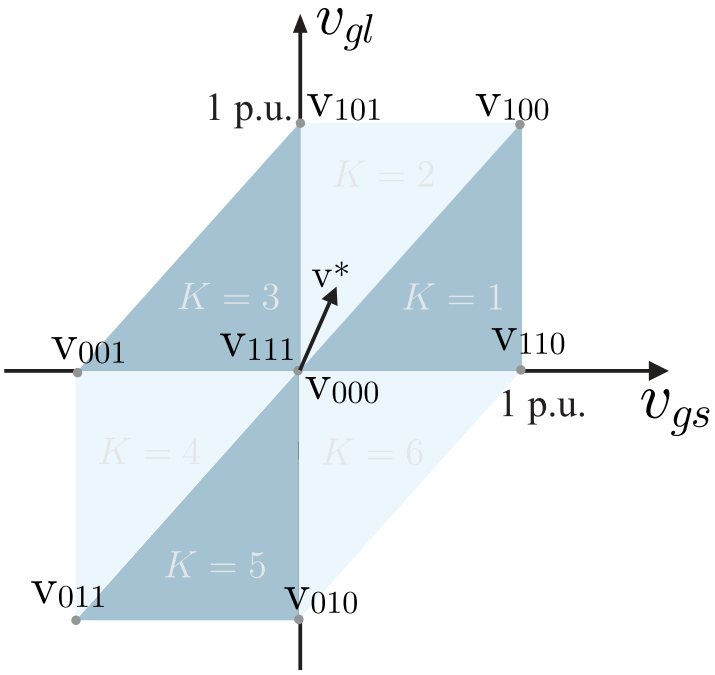


Table 4.1 – Detailing the voltage vectors in plane and the vector sequence applied for each sector.

(a) Shunt and series converter voltages generate in the space-vector plane for each voltage vector.

Voltage vector	v_{gs}	v_{gl}
	$E = 1$ p.u.	
$\mathbf{v}_{111}$	0	0
$\mathbf{v}_{110}$	E	0
$\mathbf{v}_{100}$	E	E
$\mathbf{v}_{101}$	0	E
$\mathbf{v}_{001}$	-E	0
$\mathbf{v}_{011}$	-E	-E
$\mathbf{v}_{010}$	0	-E
$\mathbf{v}_{000}$	0	0

(b) Vector Sequence.

Sector	Vector Sequence
	$\mathbf{v}_a \Rightarrow \mathbf{v}_b \Rightarrow \mathbf{v}_c$
$K = 1$	$\mathbf{v}_{111} \Rightarrow \mathbf{v}_{110} \Rightarrow \mathbf{v}_{100}$
$K = 2$	$\mathbf{v}_{111} \Rightarrow \mathbf{v}_{101} \Rightarrow \mathbf{v}_{100}$
$K = 3$	$\mathbf{v}_{000} \Rightarrow \mathbf{v}_{001} \Rightarrow \mathbf{v}_{101}$
$K = 4$	$\mathbf{v}_{000} \Rightarrow \mathbf{v}_{001} \Rightarrow \mathbf{v}_{011}$
$K = 5$	$\mathbf{v}_{000} \Rightarrow \mathbf{v}_{010} \Rightarrow \mathbf{v}_{011}$
$K = 6$	$\mathbf{v}_{000} \Rightarrow \mathbf{v}_{010} \Rightarrow \mathbf{v}_{110}$

- **Scalar PWM Strategy**

Since the desired reference voltages are represented as v_{gs}^* and v_{gl}^*, the reference pole voltages are given by

$$v_{l0}^* = v_{g0}^* - v_{gl}^*, \tag{4.16}$$

$$v_{s0}^* = v_{g0}^* - v_{gs}^*. \tag{4.17}$$

As can be seen, these equation can be solved if v^*_{g0} is specified. Thus, based on (4.16) and (4.17) one can rewrite

$$v^*_{l0} = v^*_{\mu} - v^*_{gl}, \tag{4.18}$$

$$v^*_{s0} = v^*_{\mu} - v^*_{gs}, \tag{4.19}$$

$$v^*_{g0} = v^*_{\mu}. \tag{4.20}$$

The voltage v^*_{μ} can be normalized introducing the general apportioning factor μ ($0 \leq \mu \leq 1$), that is,

$$v^*_{\mu} = \mu v^*_{max} + (1-\mu) v^*_{min}, \tag{4.21}$$

$$v^*_{max} = E^*/2 + \min\{v^*_{gl}, v^*_{gs}, 0\}, \tag{4.22}$$

$$v^*_{min} = -E^*/2 + \max\{v^*_{gl}, v^*_{gs}, 0\}. \tag{4.23}$$

Once calculated the reference pole voltages, the gate command of the switches are defined applying a carrier-based PWM technique.

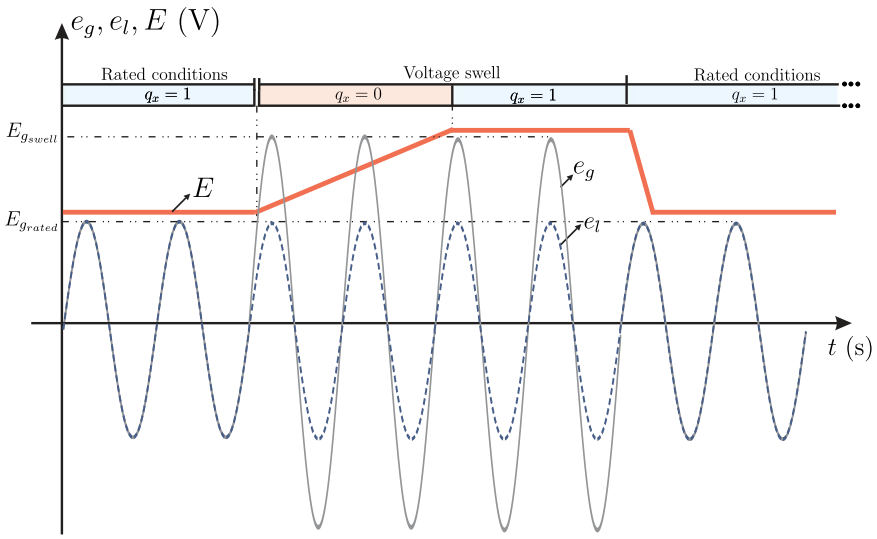
4.2.3.2 Series H-bridge Operation

In case of voltage swell events, 3L-UPQC cannot control the grid current, if the amplitude of the grid voltage is higher than the dc-link voltage. In this scenario, this converter commonly operates with high dc-link voltage to compensate swells. For the proposed 3LS-UPQC, the bidirectional switch, q_x, in the leg s allows changing the three-leg converter to a simple series two-leg converter. Here, it is proposed that at the moment when the voltage swell starts, the switch is opened. At this moment, the swell compensation will make the dc-link capacitor to charge, increasing its dc-link voltage until reaching a value higher than the grid voltage amplitude. At this time, the switch is closed and the topology returns to operate as an ac-dc-ac converter. Note that while the converter operates as an h-bridge, the load voltage also remains compensated, moreover the grid current becomes equal to the load current. A idealized representation of a voltage swell transient 4.5(a).

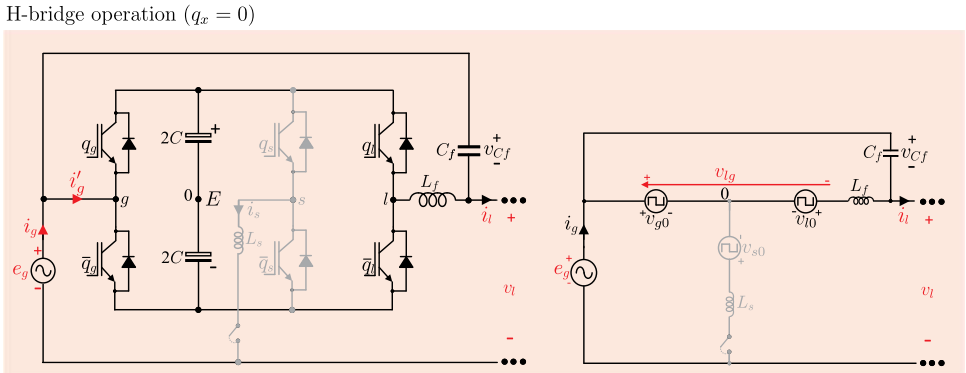
Therefore, this operation is considered only when q_x is opened and the circuit becomes an h-bridge converter composed by legs g and l, as presented in Fig. 4.5(b). In open loop control, the series converter reference voltage (v^*_{gl}) can be defined by $v^*_{gl} = e_g$

- v_l^* to compensate the load voltage e_l. In this way, the gate command for the switches q_g–$\bar{q}_g$ and q_l–$\bar{q}_l$ are defined applying a carrier-based PWM modulation strategy. Since $|v_{gl}| \leq E$ (= 1 pu), the load voltage can be compensated during the disturbance if the voltage swell is limited to 2 pu. Fig. 4.6(a-c) present, respectively, the fasorial diagram considering the series h-bridge operation and the ac-dc-ac operation during and after the swell event.

Figure 4.5 – Operation under a voltage swell. (a) Idealized representation of a voltage swell transient. (b) Topological state for compensating swells.



(a)



(b)

4.2.4 Control System

Fig. 4.7(a) shows the control diagram of the proposed structure. The dc-link voltage is regulated by a conventional (PI) controller that can generates the reference of the grid current amplitude I_g^* or of the shunt compensation current amplitude I_s^*. If i_s is considered, since $i_s = i_g$ - i_l, the portion referred to the active, harmonic and reactive part of the load current need to be measured to generate the reference of the shunt compensation current.

Figure 4.6 – Phasor Diagram. (a) Series h-bridge operation. (b) Ac-dc-ac operation during the swell event. (c) Ac-dc-ac operation after the swell event.

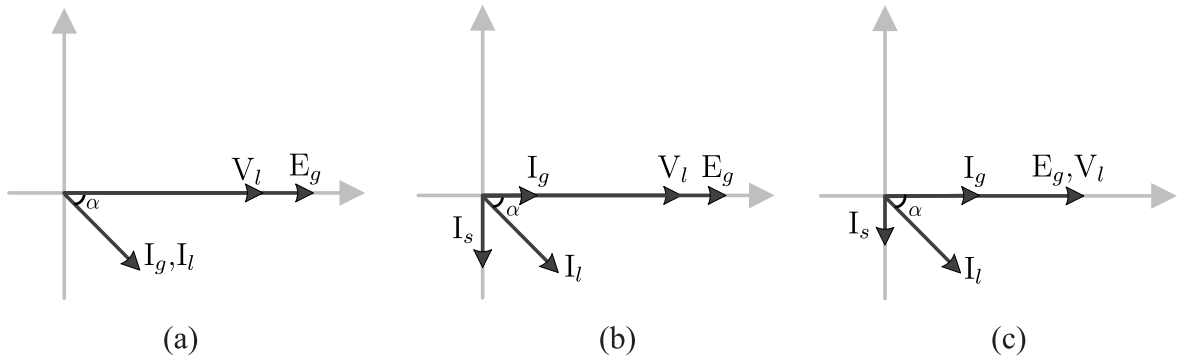
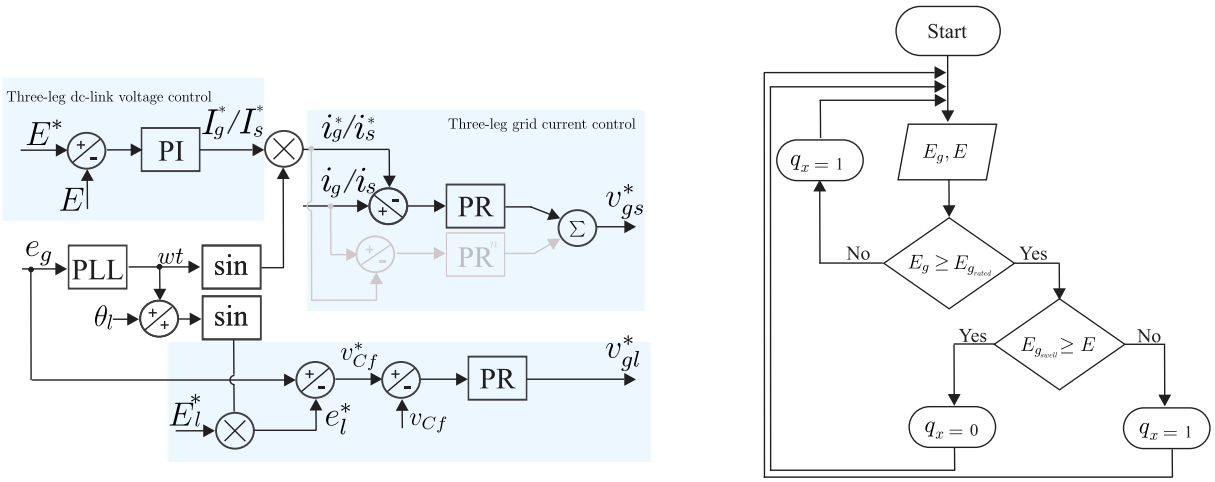


Figure 4.7 – Control system. (a) Control diagram to generate the shunt and series reference voltages. (b) Flowchat of the q_x operation.



In this way, the grid current was considered in the implementation of this control. The angle of the grid voltage (θ_g) is obtained using a single-phase phase-locked loop (PLL). Thus, it is possible to synchronize i_g with e_g, which allows a grid power factor close to the unit. To define the shunt converter reference voltage v^*_{gs}, a resonant controller (JACOBINA et al., 2001) is used. In the case of a nonlinear load, an additional PR block needs to be tuned for each harmonic. Therefore, PR^n blocks receive the error i_g-i^*_g and provide the amplitude of the respective harmonic.

Taking into account that the grid voltage is monitored, the load voltage control is implemented considering two operation modes: 1) in rated conditions or with voltage sags; 2) with voltage swell. In the first operation mode ($q_x = 1$), the converter operates as ac-dc-ac converter and the closed-circuit path -e_g + v_{Cf} + e_l = 0, is considered. In this way, the output filter reference voltage (v^*_{Cf}) is obtained from the aforementioned voltage path with the grid voltage e_g and the reference load voltage e^*_l defined. The PR block sets the series converter reference voltage v^*_{gl} to control the load voltage e_l. The second

operation mode is considered when q_x is opened and the converter operates as an h-bridge converter. In this scenario, the load voltage is compensated considering the same voltage path. Fig. 4.7(b) shows the operation of q_x taking into account the monitoring of the grid voltage amplitude.

4.2.5 Results

The feasibility of the proposed 3LS-UPQC is demonstrated through simulation and experimental results in closed-loop control. The setup used in the tests consists of semiconductor power devices from SEMIKRON, with IGBTs and gate drivers SKH22, as well as a DSP TMS320F28335 from Texas Instruments.

4.2.5.1 Simulation Results

Simulation results were performed to demonstrate the capability of the proposed topology to operate as a UPQC, ensuring series and shunt compensation. Unless made clear otherwise, the parameters used in these tests are presented in Table 4.2 (Nonlinear load I). Initially, the operation of the proposed converter was verified with grid voltage and load current disturbances simultaneously. For the grid voltage, third (10%), fifth (5%), and seventh (2%) order harmonics were considered. As for the load, the converter fed a nonlinear load with approximately 70% of harmonic distortion and 1.9 kVA. Figs. 4.8, 4.9, and 4.10 differ from each other by operating, respectively, with the grid voltage under rated conditions, 30% of voltage sag, and 30% of voltage swell, respectively. Note that in the three scenarios, the converter provides grid power factor control, load voltage compensation, and dc-link voltage regulation. It is also important to highlight that grid current achieved a THD less than 5% in the three scenarios analyzed.

Next, the feasibility of the proposed system was verified over grid voltage and load current transients. Table 4.2 presents the parameters used in these tests (RL load and Nonlinear load 2). For the series tests, an RL load with an inductive power factor of 0.97 was considered and for the shunt tests, a typical single-phase full-bridge rectifier with a harmonic distortion of approximately 27% was used as a nonlinear load. Firstly, for the shunt tests, Fig. 4.11 shows a load transient, where the active power is increased by about 70%. As can be seen, the control strategy guarantees the dc-link voltage regulation and a sinusoidal grid current in phase with the grid voltage. The performance of the series compensation has been demonstrated taking into account events of voltage swell and sag. Fig. 4.12 shows the behavior of the proposed topology in operation under nominal conditions and with 30% of voltage swell. As it can be seen, under nominal conditions (t = 1 s to 1.5 s) e_l is compensated. At t = 1.5 s, 30% of voltage swell is applied to the system. At this moment, the switch q_x is opened and the converter starts to operate as an h-bridge converter. During this transient, the load voltage remains compensated. Approximately

after t = 1.625, q_x is closed as the dc-link voltage becomes higher than the amplitude of the grid voltage. In this way, the converter returns to operate as an ac-dc-ac converter. After the voltage swell, the dc-link voltage can reach its nominal value again, so that the converter can operate under nominal conditions with a high modulation index. Fig. 4.13 depict the load voltage compensation during an event of 30% of voltage sag. One can see that e_l remains at its nominal value during this disturbance.

Table 4.2 – Parameters used in simulations and experimental tests.

Parameter		Value
Grid voltage	e_g	110 V rms 77 V rms 143 V rms
Load reference voltage	e_l^*	110 V rms
Switching frequency	f_s	10 kHz
Dc-link capacitor	C	2.2 mF
Three-leg shunt inductance	L_s	5 mH
Series filter inductance	L_f	2 mH
Series filter capacitance	C_f	18 μH
Series filter dump resistance	R_f	10 Ω
RL Load		
Dc-link voltage	E	170 V
Load power factor	$\cos(\delta_l)$	0.97 (lagging)
Load power	P_l	0.5 kW
Nonlinear load I		
Dc-link voltage	E	280 V
Load power	P_l	1.5 kW
Load current THD	THD_{il}	70%
Nonlinear load II		
Dc-link voltage	E	170 V
Load power	P_l	0.6/1.1 kW
Load current THD	THD_{il}	27%

4.2.5.2 Experimental Results

Experimental results in steady-state and transient are presented to validate the series and shunt capability of the proposed converter. The parameters used are presented in Table 4.2. Fig. 4.14 shows steady state results under rated conditions for the grid voltage and current, as well as load voltage and current. In this scenario, the converter feeds a nonlinear load with 25% of harmonic distortion. Besides since the grid voltage does not have harmonics it was considered $v_{gl} = 0$. The experimental THD of the grid was measured, reaching a THD of 1.68%.

Fig. 4.15 shows a transient in the active power of the system at about 70%. The dc-link voltage, grid current, shunt compensation current, and load current are shown before, during, and after the transient. Notice that the dc-link voltage is adequately

Figure 4.8 – Simulation results of the proposed converter under nominal conditions. (a) Grid voltage with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic and grid current. (b) Load voltage and Load current. (c) Shunt compensation current. (d) Dc-link voltage E.

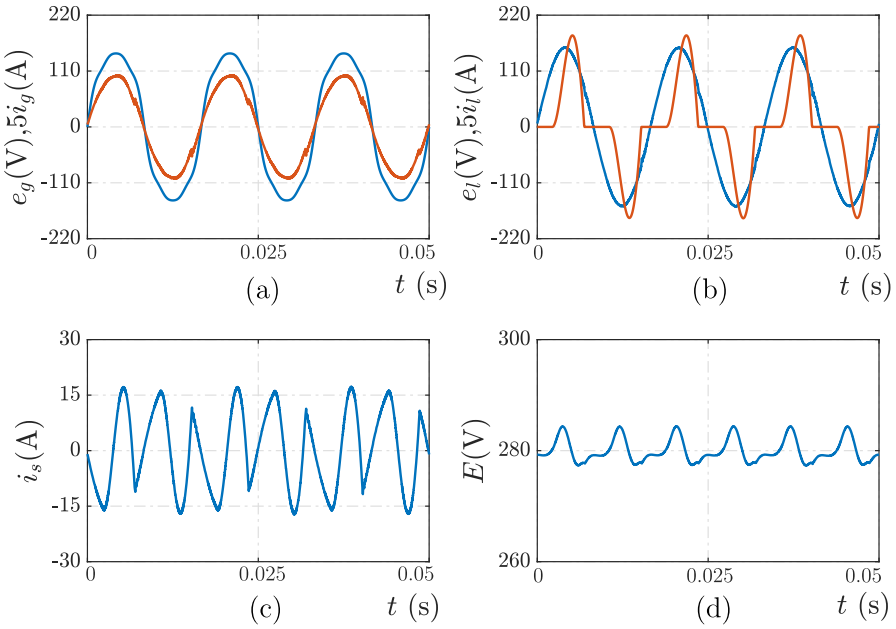
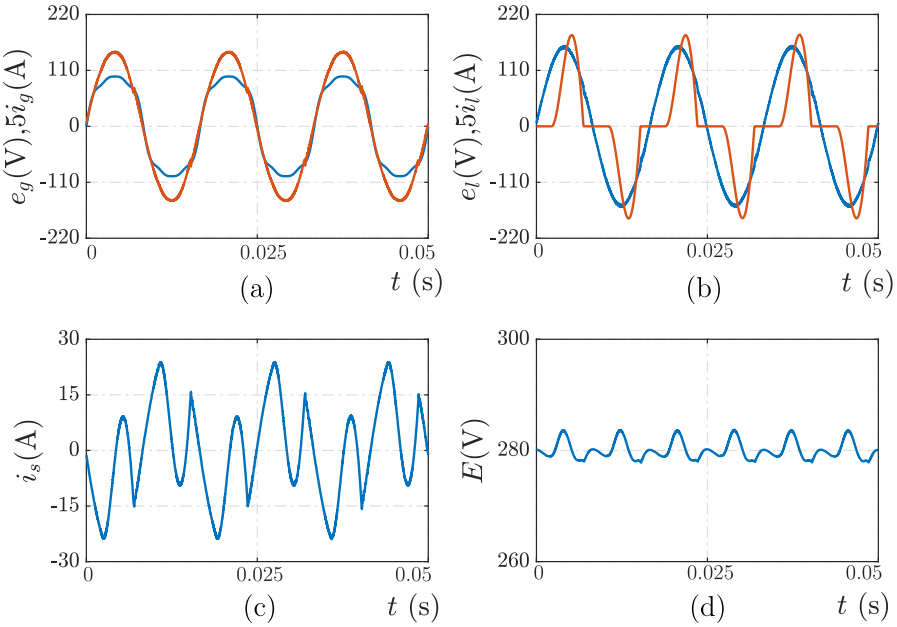


Figure 4.9 – Simulation results of the proposed converter under 30% of grid voltage sag. (a) Grid voltage with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic and grid current. (b) Load voltage and Load current. (c) Shunt compensation current. (d) Dc-link voltage E.



regulated. The increase in the load current generates an increase in the grid current to adjust the dc-link voltage.

Figs. 4.16 and 4.17 depict experimental results of the proposed converter operating with sag and swell transients. The dc-link voltage, grid voltage, load voltage, and series converter voltage are depicted. Fig. 4.16 demonstrates the capability of the proposed

Figure 4.10 – Simulation results of the proposed converter under 30% of grid voltage swell. (a) Grid voltage with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic and grid current. (b) Load voltage and Load current. (c) Shunt compensation current. (d) Dc-link voltage E.

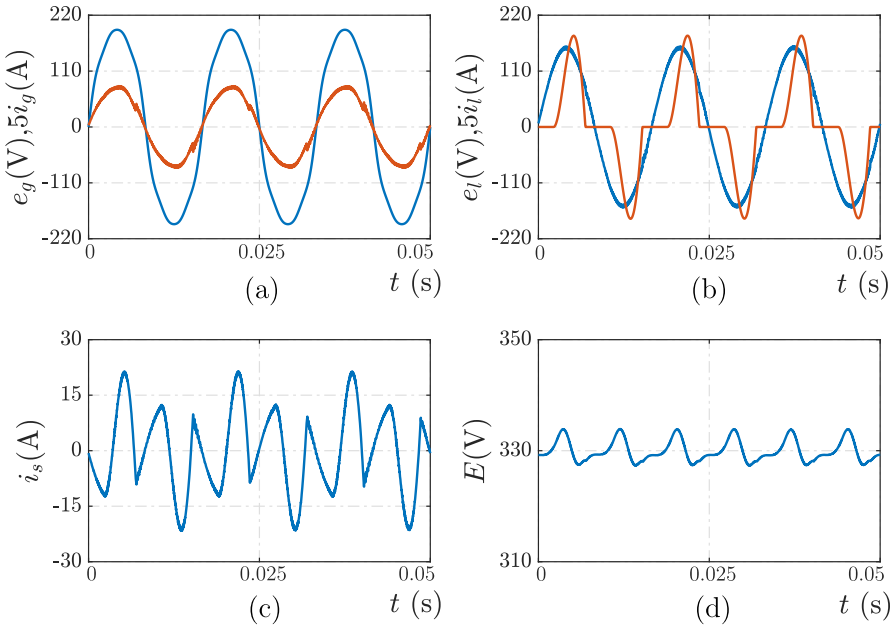


Figure 4.11 – Simulation results with nonlinear load. Transient caused by a load power increased from P_l = 600 W to P_l = 1.1 kW.

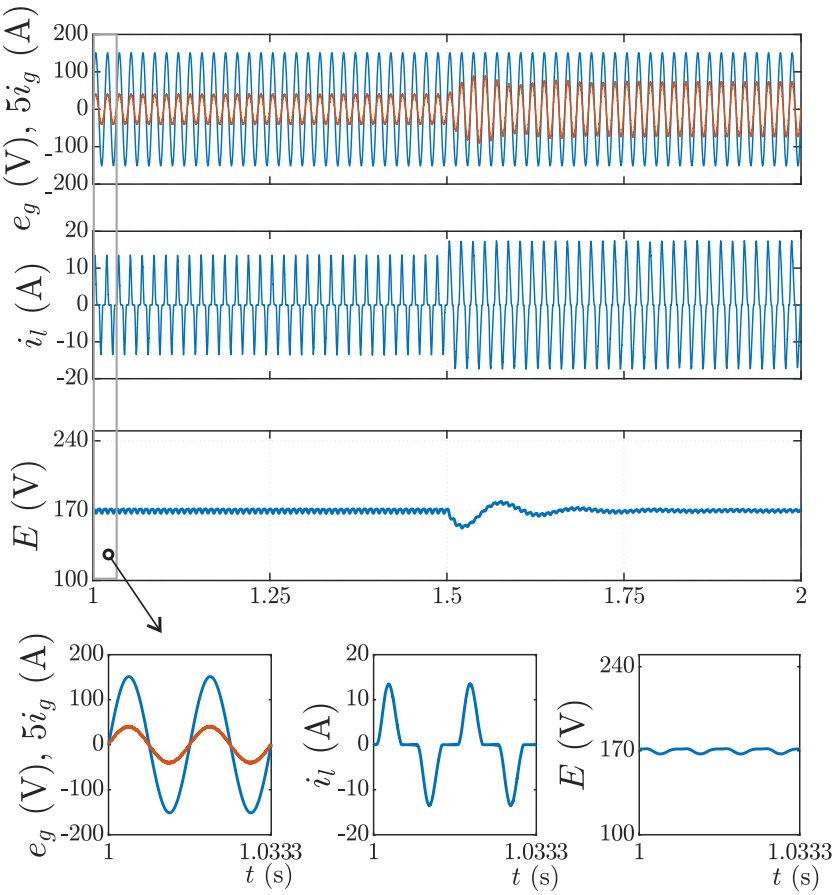


Figure 4.12 – Simulation results with linear load with load power $P_l = 500$ W under a voltage swell of 30%.

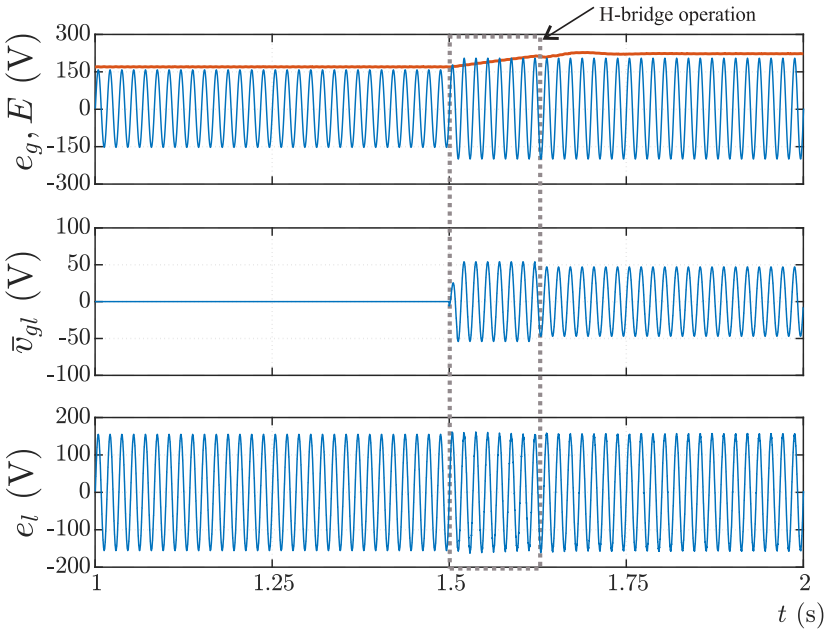
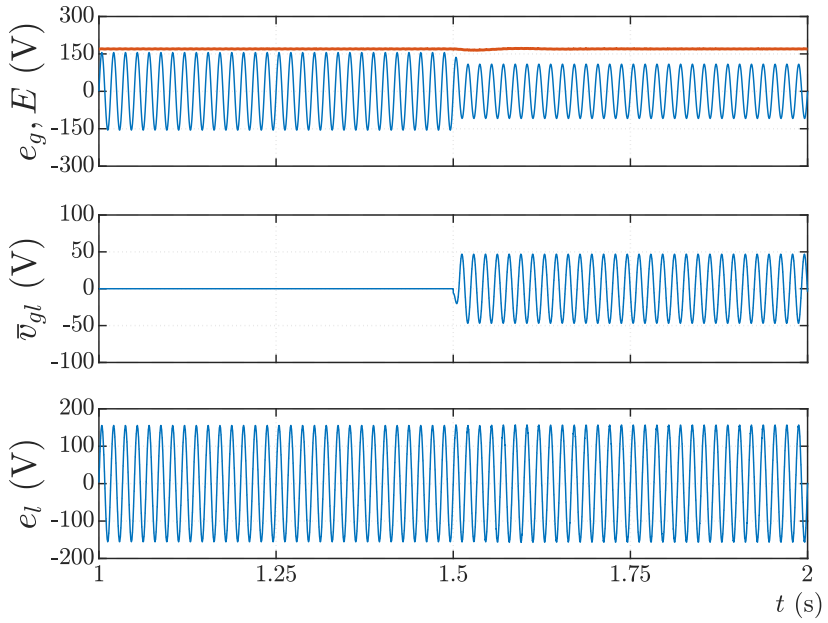
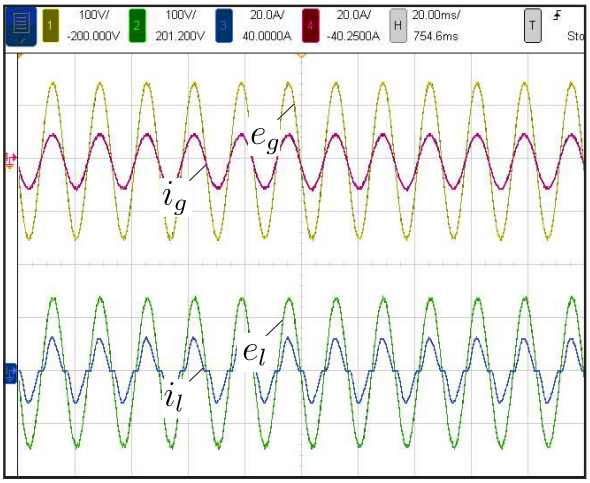


Figure 4.13 – Simulation results with linear load with load power $P_l = 500$ W under a voltage sag of 30%.

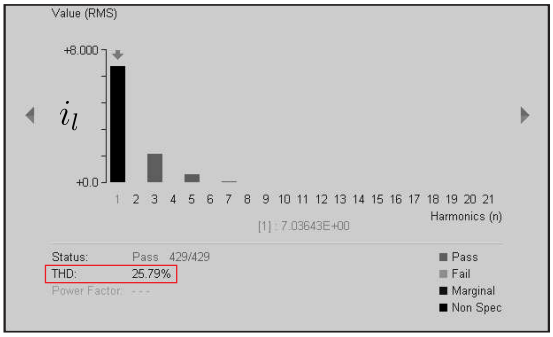


converter to compensate 30% of voltage swell. When the disturbance occurs, q_x is opened, and the converter operates as an h-bridge converter until the dc-link voltage E becomes higher than the amplitude of the grid voltage. At this moment, the converter returns to operate as an ac-dc-ac converter. One can note that the load voltage remains always compensated. Lastly, Fig. 4.17 shows a voltage sag transient in the grid voltage of 30%. The load voltage remains compensated.

Figure 4.14 – Experimental results in steady state for THD measurement of the grid and load currents for $v_{gl} = 0$. (a) Grid voltage (e_g), grid current (i_g), load voltage (e_l), and load current (i_l). (b) THD of the load current. (c) THD of the grid current.



(a)



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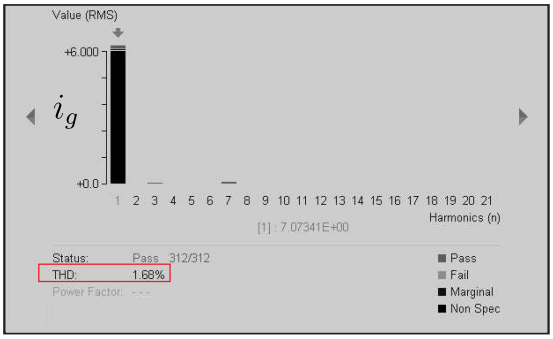
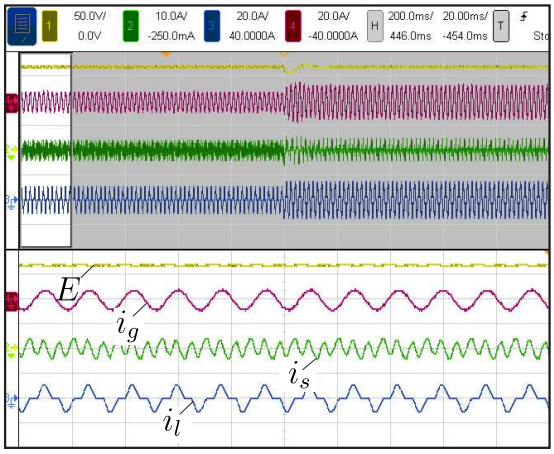
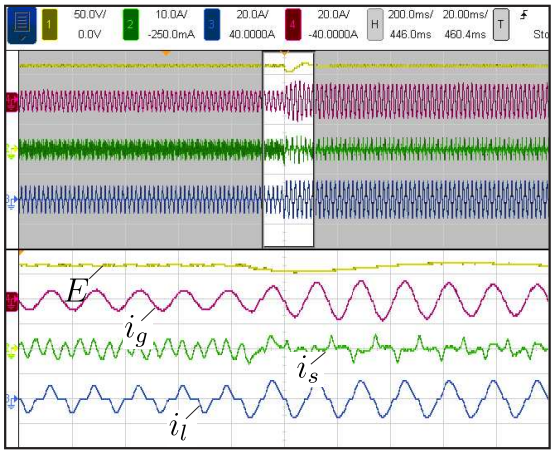


(c)

Figure 4.15 – Experimental results with transient - Increase in the active power of 70%. (a) Dc-link voltage (E), grid current (i_g), shunt compensation current (i_s), and load current (i_l) with zoomed view before the load transient. (b) Dc-link voltage (E), grid current (i_g), shunt compensation current (i_s), and load current (i_l) with zoomed view during the load transient (c) Dc-link voltage (E), grid current (i_g), shunt compensation current (i_s), and load current (i_l) with zoomed view after the load transient.



(a)



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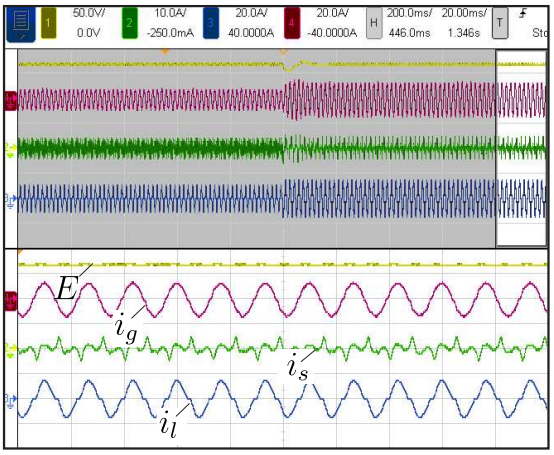
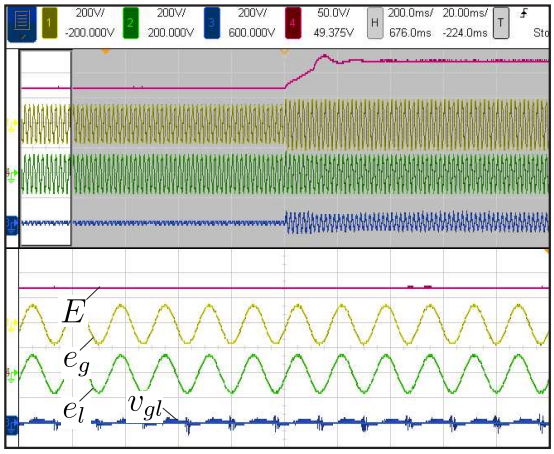
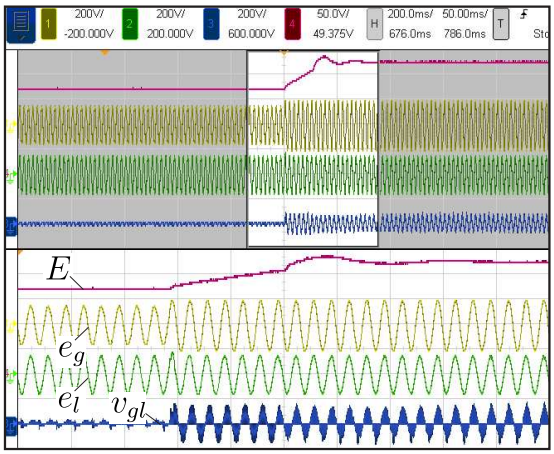


(c)

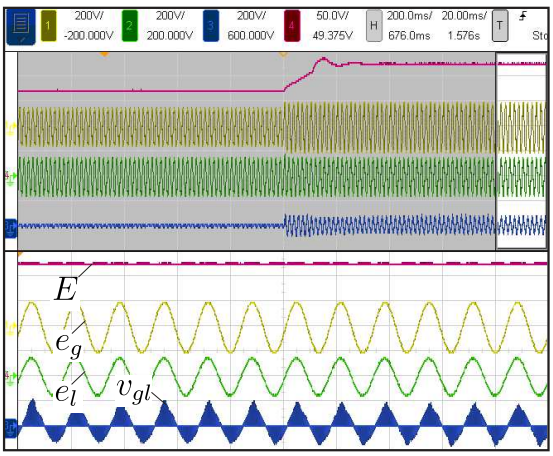
Figure 4.16 – Experimental results - Grid voltage swell of 30%. (a) Dc-link voltage (E), grid voltage (e_g), load voltage (e_l), and series converter voltage (v_{gl}) with zoomed view before the transient. (b) Dc-link voltage (E), grid voltage (e_g), load voltage (e_l), and series converter voltage (v_{gl}) with zoomed view during the transient. (c) Dc-link voltage (E), grid voltage (e_g), load voltage (e_l), and series converter voltage (v_{gl}) with zoomed view after the transient.



(a)

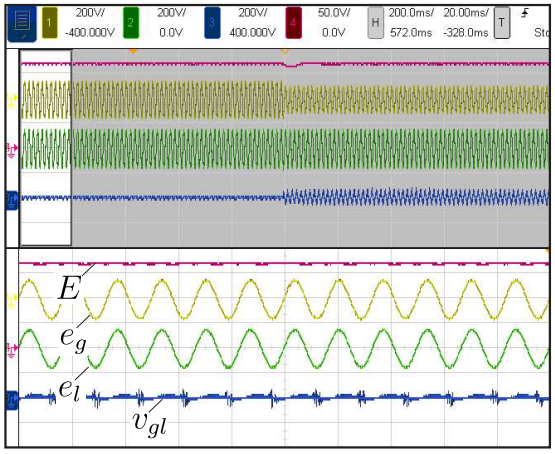


(b)

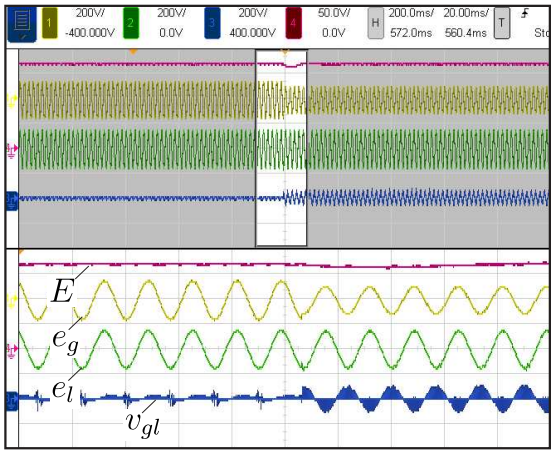


(c)

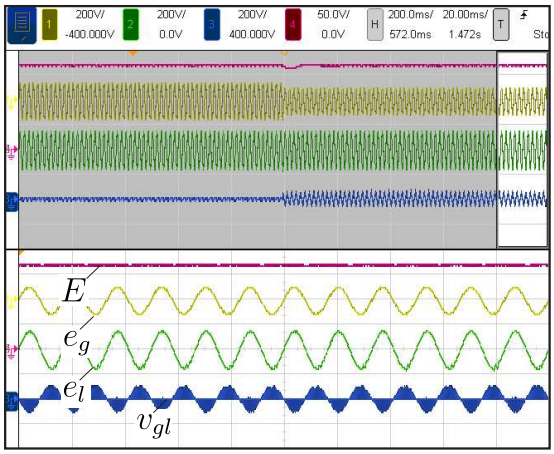
Figure 4.17 – Experimental results - Grid voltage sag of 30%. (a) Dc-link voltage (E), grid voltage (e_g), load voltage (e_l), and series converter voltage (v_{gl}) with zoomed view before the transient. (b) Dc-link voltage (E), grid voltage (e_g), load voltage (e_l), and series converter voltage (v_{gl}) with zoomed view during the transient. (c) Dc-link voltage (E), grid voltage (e_g), load voltage (e_l), and series converter voltage (v_{gl}) with zoomed view after the transient.



(a)



(b)



(c)

4.3 Five-Leg Converter Based on Three-Leg and Standby Converter (SB-3LS-UPQC)

In this section, a transformerless single-phase unified power quality conditioner (UPQC) based on three-leg and standby converters is proposed. The system consists of a two-leg module series-connected to a three-leg module. The proposed control system provides shunt and series compensation and can be designed to decouple the operation under nominal and grid voltage sags conditions of the transients of the grid voltage swells. In addition, a low standby power consumption and a new decoupling method to compensate for voltage swells using the two-leg module are proposed. This approach avoids issues related to the operation without grid power factor correction and difficulties in reconfiguring under highly inductive loads in the 3LS-UPQC configuration. The system model, the scalar PWM technique, the applied standby concept, and the overall control system strategy are discussed. Simulations and experimental results are presented to evaluate the proposed system's feasibility and the design methodology's correctness.

4.3.1 System Model

Fig. 4.18 presents the proposed transformerless single-phase UPQC based on three-leg and standby converters, named here SB-3LS-UPQC. The configuration is composed by a single-phase grid and load voltage (e_g and e_l), a two-leg module (standby converter), a three-leg module, inductor and capacitor filters (L_a, C_l, and L_l), and two dc links (C_s, C). Pairs $q_j - \bar{q}_j$, with $j = \{s1, s2, g, a, l\}$ are complementary and the switching conduction state is represented by $q_j = 1$ when the switch is closed and $q_j = 0$ when is opened. Fig. 4.19 presents the simplified equivalent circuit of the proposed configuration, where v_{se_s} is the series converter voltage of the two-leg module, v_{sh} and v_{se} are the series and shunt converter voltage of the three-leg module, respectively, and v_{Cf} and e_l are the output filter voltage and load voltage, respectively; i_g, i_l, and i_a are the grid current, load current, and shunt compensation current, respectively. From Kirchhoff's voltage law, the voltages v_{se_s}, v_{se}, v_{sh}, and e_l are given, respectively, by

$$v_{se_s} = v_{s10s} - v_{s20s}, \tag{4.24}$$

$$v_{se} = v_{g0} - v_{l0}, \tag{4.25}$$

$$v_{sh} = v_{g0} - v_{a0}, \tag{4.26}$$

$$e_l = e_g - v_{C_f}, \tag{4.27}$$

where v_{s10s}, v_{s20s}, v_{g0}, v_{l0}, and v_{a0} are the pole voltages of the converter, which can be denoted for the two- and three-leg modules, respectively, as

$$v_{j0s} = (2q_j - 1)\frac{E_s}{2}, \tag{4.28}$$

$$v_{j0} = (2q_j - 1)\frac{E}{2}, \tag{4.29}$$

where E_s and E are the dc-link voltages of the two- and three-leg converters, respectively.

Figure 4.18 – Proposed SB-3LS-UPQC configuration.

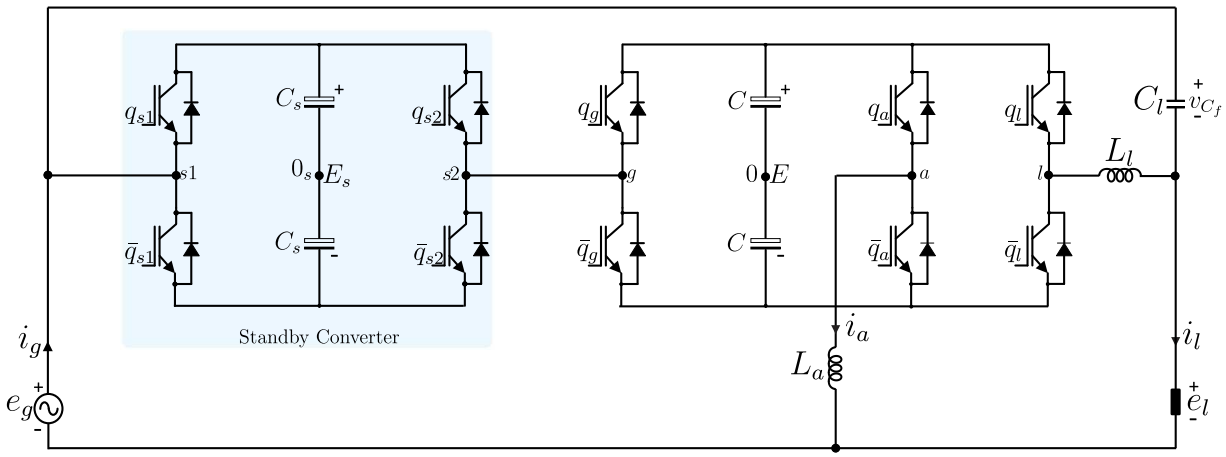
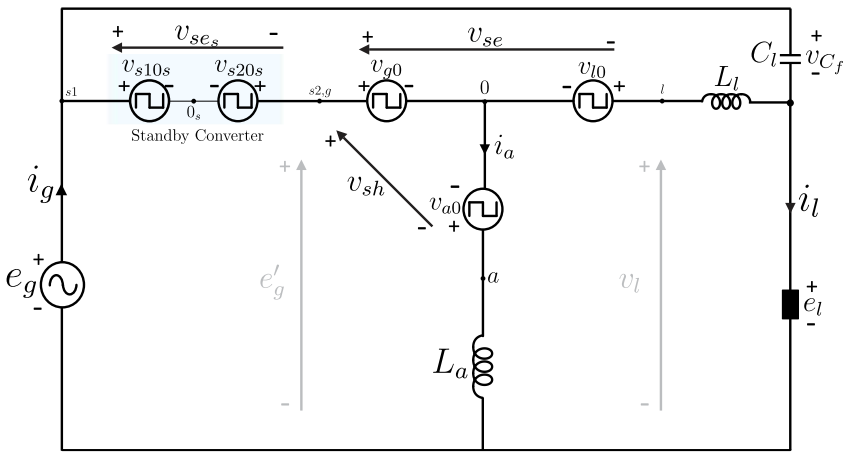


Figure 4.19 – Equivalent circuit.



4.3.2 PWM Strategy

In this paper, two PWM strategies are designed to control the proposed SB-3LS-UPQC. In the following, the superscript * denotes the reference variables.

4.3.2.1 Three-leg Converter and Standby Operation

The PWM strategy discussed in this section considers scenarios with rated or grid voltage sag conditions. In both cases, the three-leg module is responsible for compensating the grid current and load voltage, while the two-leg module operates with low power consumption. This approach allows partial decoupling of the PWM strategy for both modules. Therefore, the PWM strategy for the three-leg module is first designed separately.

A scalar PWM is developed to control the three-leg converter. Assuming that the desired series and shunt reference voltages are defined by the control strategy, the reference pole voltages for the three-leg module are given by

$$v_{l0}^{*} = v_{g0}^{*} - v_{se}^{*} \tag{4.30}$$

$$v_{a0}^{*} = v_{g0}^{*} - v_{sh}^{*} \tag{4.31}$$

These equations can be solved for v_{l0}^{*} and v_{a0}^{*} if v_{g0}^{*} is known. In this way, v_{g0}^{*} can be defined considering the limits of v_{se}^{*} and v_{sh}^{*}, i.e., taking into account the following dc-link voltage requirements,

$$v_{g0}^{*} = \frac{v_{\max}^{*} + v_{\min}^{*}}{2} \tag{4.32}$$

where

$$v_{\max}^{*} = E^{*}/2 + \min\{v_{se}^{*}, v_{sh}^{*}, 0\} \tag{4.33}$$

$$v_{\min}^{*} = -E^{*}/2 + \max\{v_{se}^{*}, v_{sh}^{*}, 0\} \tag{4.34}$$

The standby operation proposed here aims a low power consumption of the two-leg module to ensure only the regulation of the dc-link voltage E_s. Therefore, a hysteresis voltage regulation is used, which receives as inputs the measured voltage E_s, the reference voltage E_s^{*}, the grid current i_g, and the upper ($u_b = E_s^{*} + \gamma$) and lower ($l_b = E_s^{*} - \gamma$) hysteresis bands. The technique for regulating E_s is shown in Fig. 4.20 in the form of a flowchart. Notice that, the legs s_1 and s_2 are initially clamped ($v_{s10s}^{*} = v_{s20s}^{*} = E_s^{*}/2$). When the dc-link voltage E_s needs to be charged or discharged, a percentage of $v_{se_s}^{*}$ (kE_s^{*}) is considered to define the pulse width applied to ensure regulation of E_s. In this way, the reference pole voltages of the two-leg module can be defined as follows

$$v_{s10s}^{*} = \frac{v_{se}^{*}}{2} \tag{4.35}$$

$$v^*_{s20s} = -\frac{v^*_{se}}{2} \tag{4.36}$$

Notice that the reference voltages v^*_{sh} and v^*_{se} of the three-leg module are affected when the two-leg module switches. To compensate for this effect, the reference pole voltage v^*_{g0} must be corrected, i.e. $v^*_{g0} = v^*_{g0} - v^*_{se_s}$. A standard carrier-based PWM strategy was used to define the states of the switches.

4.3.2.2 Series Active Filter Operation

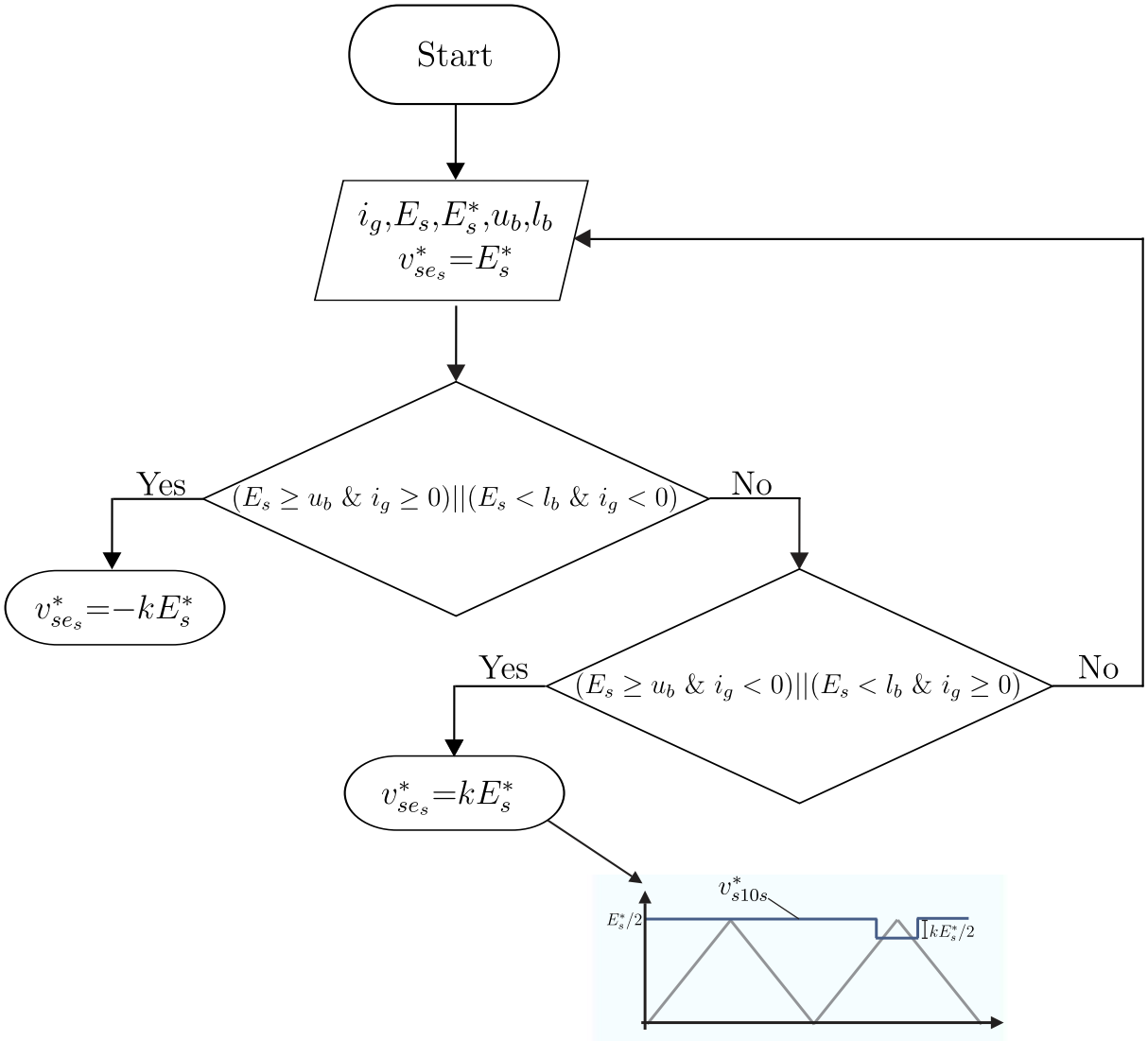
To compensate for disturbances related to grid voltage swells, single-phase three-leg converters based on shared-leg must be designed to operate with a low modulation index, which also affects the operation under rated and sag conditions in terms of efficiency and harmonic distortion. In the proposed SB-3LS-UPQC, the two-leg module changes its mode of operation to allow series compensation and operation with a low modulation index only under swell conditions.

Here, it is proposed that at the moment when the voltage swell starts, the two-leg module operates as a series active filter in open loop. In this way, $v^*_{se_s} = e_g - e'^*_g$ (see Fig. 4.19(b)), where e'^*_g is the input reference voltage of the three-leg module under this operation mode. During the swell compensation the dc-link voltage E_s will be charged, however the fundamental component of the voltage e'_g is corrected at each time step. During the increase of E_s, the dc-link reference voltage of the three-leg module (E^*) will be set to a new reference voltage capable of compensating the disturbance, i.e, until it reaches a value higher than the amplitude of the grid voltage. At this moment, the two-leg module returns to operate in standby mode and the three-leg converter starts to compensate the disturbance in the grid. During this transient the load voltage remains compensated.

4.4 Control System

The control diagram of the configuration SB-3LS-UPQC is shown in Fig. 4.21. First, the dc-link voltage of the three-leg module (E) is regulated by a proportional-integral (PI) controller, represented by R_E block. This block gives the amplitude of the reference grid current, I^*_g. The phase angle of the grid voltage, e_g, is obtained using a single-phase phase-locked loop (PLL), which allows to synchronize the reference grid current, i^*_g, with the fundamental frequency of the grid voltage. The shunt converter reference voltage, v^*_{sh}, is generated by a resonant controller, identified here as R_{i_g} block. This loop control has the capability to compensate only reactive currents. To mitigate harmonics from the load, additional PRs blocks need to be added to the reference of the fundamental component (50/60 Hz).

Figure 4.20 – Flowchart for the regulation of E_s in the standby mode.

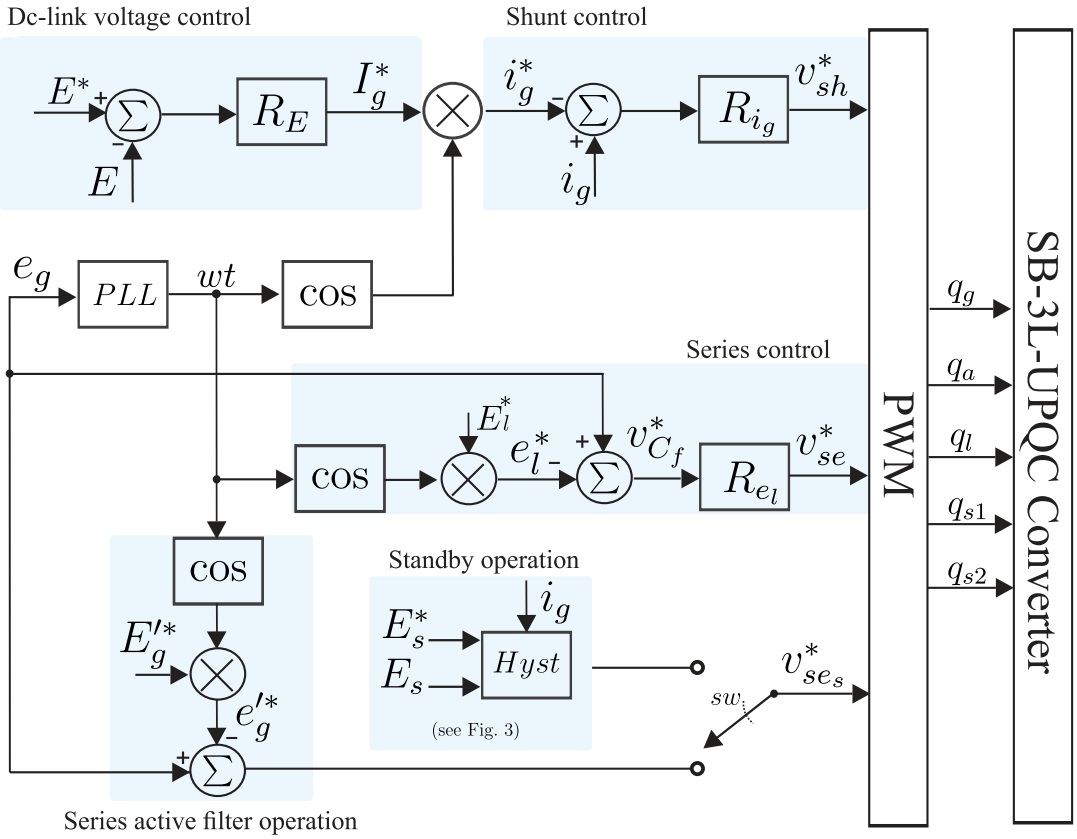


To determine if there is a voltage swell, the grid voltage is monitored. In case of voltage swell, $sw = 1$. For voltage sags or rated conditions, $sw = 0$. When $sw = 0$, the proposed system operates with the two-leg module in standby mode and the three-leg module is responsible for compensating the grid current and load voltage. When $sw = 1$, the series active filter mode is turned on, which allows the dc-link reference voltage of the three-leg converter to be changed to withstand the transients. To control the load voltage, the closed loop -e_g + v_{Cf} + e_l = 0 is considered. Therefore, the output filter reference voltage, v_{Cf}^*, can be calculated considering e_g and e_l^* known. The R_{e_l} block, also a resonant controller, sets the series converter reference voltage, v_{se}^*, to control the load voltage, e_l.

4.4.1 Results

The capability of the proposed SB-3L-UPQC is demonstrated through simulation and experimental results. The setup used in the tests consists of semiconductor

Figure 4.21 – Control diagram.



power devices from SEMIKRON, with IGBTs and gate drivers SKH23, as well as a DSP TMS320F28335 from Texas Instruments.

4.4.1.1 Simulation Results

Simulation tests were performed to validate the performance of the proposed structure as a UPQC system. First, the functionality of the proposed converter was confirmed under simultaneous grid voltage and load current disturbances. Unless made clear otherwise, the parameters used in these tests are presented in Table 4.3 (Nonlinear load). The grid voltage disturbances included third (10%), fifth (5%), and seventh (2%) order harmonics. These tests used a nonlinear load with approximately 70% harmonic distortion and 1.9 kVA. Figures 4.22, 4.23, and 4.24 show different operating conditions: grid voltage under nominal conditions, 30% voltage sag, and 30% voltage swell, respectively. It can be observed that the converter maintains grid power factor regulation, load voltage compensation, and dc-link voltage regulation in all three scenarios. Additionally, it was verified that the grid current achieved a THD of less than 5% in each scenario analyzed.

Next, simulation results were presented in Figures 4.25, 4.26, and 4.27 to demonstrate the capability of the proposed system to compensate for transients such as reactive load currents, as well as voltage sags and swells in the grid. The parameters considered

for these tests are presented in Table 4.3 (RL load). Fig. 4.25 depicts the behavior of the SB-3LS-UPQC configuration operating under rated voltage and with 50% of voltage swell. Under rated conditions (t = 0.5 s to 1 s) the converter operates with unity power factor on the grid side. Moreover, the load voltage e_l is compensated. At t = 1.0 s, 50% of voltage swell is applied to the system. At this moment, the two-leg module starts to operate as a series active filter (see its average value, $\bar{v}_{se_s}$) to compensate the input voltage of the three-leg module (e_l'). At the same moment, the dc-link reference voltage of the three-leg module (E^*) is updated to handle the voltage swell. When the voltage E reaches its new reference value, the two-leg module switches back to standby mode. Note that the load voltage remains compensated. After the voltage swell transient, the dc-link voltage of the three-leg module can return to its nominal value, allowing operation with a high modulation index. Fig. 4.26 presents the behavior of the proposed converter under 50% of voltage sag. Notice that when the disturbance starts (t = 1 s), the series converter voltage (v_{se}) produces a waveform with voltage amplitude needed to compensate the load voltage e_l. Observing that the dc-link voltage remains regulated since the grid current keeps controlled during the transient. Lastly, Fig. 4.27 shows a transient caused by a load power increased from P_l = 536 W to P_l = 770 W. The increase in the load current generates an increase in the grid current, which allows to regulate the dc-link voltage.

Table 4.3 – Parameters used in simulations and experimental tests.

Parameter		Value
Grid voltage	e_g	110 V rms 55 V rms 165 Vrms
Load reference voltage	e_l^*	110 V rms
Switching frequency	f_s	10 kHz
Dc-link capacitor	C, C_s	2.2 mF
Three-leg shunt inductance	L_s	5 mH
Series filter inductance	L_f	2 mH
Series filter capacitance	C_f	18 μH
Series filter dump resistance	R_f	10 Ω
RL Load		
Dc-link voltage	E, E_s	180/180 V
Load power factor	$\cos(\delta_l)$	0.97 (lagging)
Load power	P_l	536/770 W
Nonlinear Load		
Dc-link voltage	E, E_s	280/170 V
Load Power	P_l	1.5 kW
Load current THD	THD_{il}	70%

Figure 4.22 – Simulation results of the proposed converter under nominal conditions. (a) Grid voltage with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic and grid current. (b) Load voltage and load current. (c) Three-leg module shunt compensation current (i_s). (d) Dc-link voltage of the three-leg module (E). (e) Shunt compensation current (i_h). (f) Dc-link voltage of the shunt module (E_h).

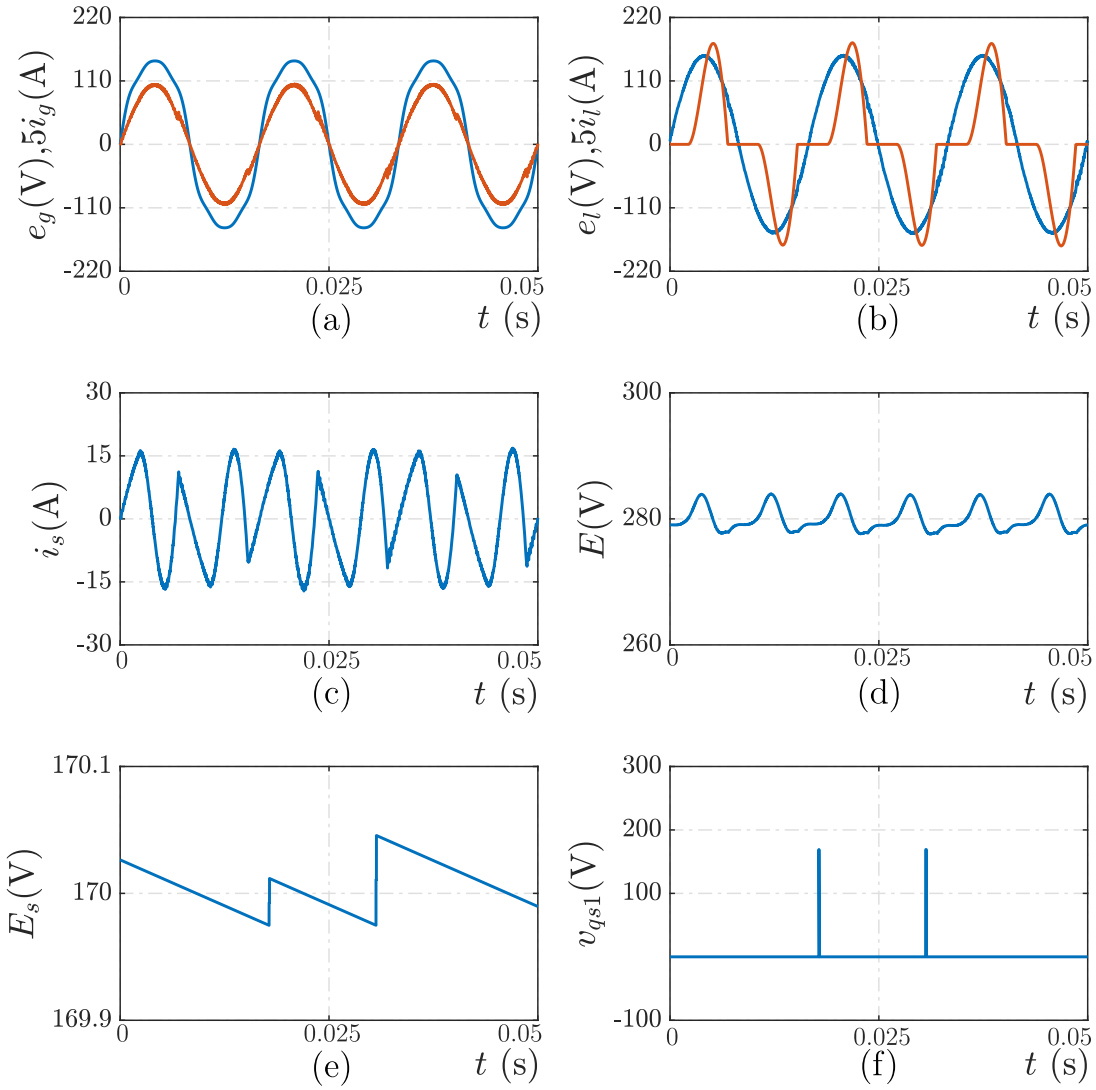


Figure 4.23 – Simulation results of the proposed converter under 30% of grid voltage sag. (a) Grid voltage with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic and grid current. (b) Load voltage and load current. (c) Three-leg module shunt compensation current (i_s). (d) Dc-link voltage of the three-leg module (E). (e) Shunt compensation current (i_h). (f) Dc-link voltage of the shunt module (E_h).

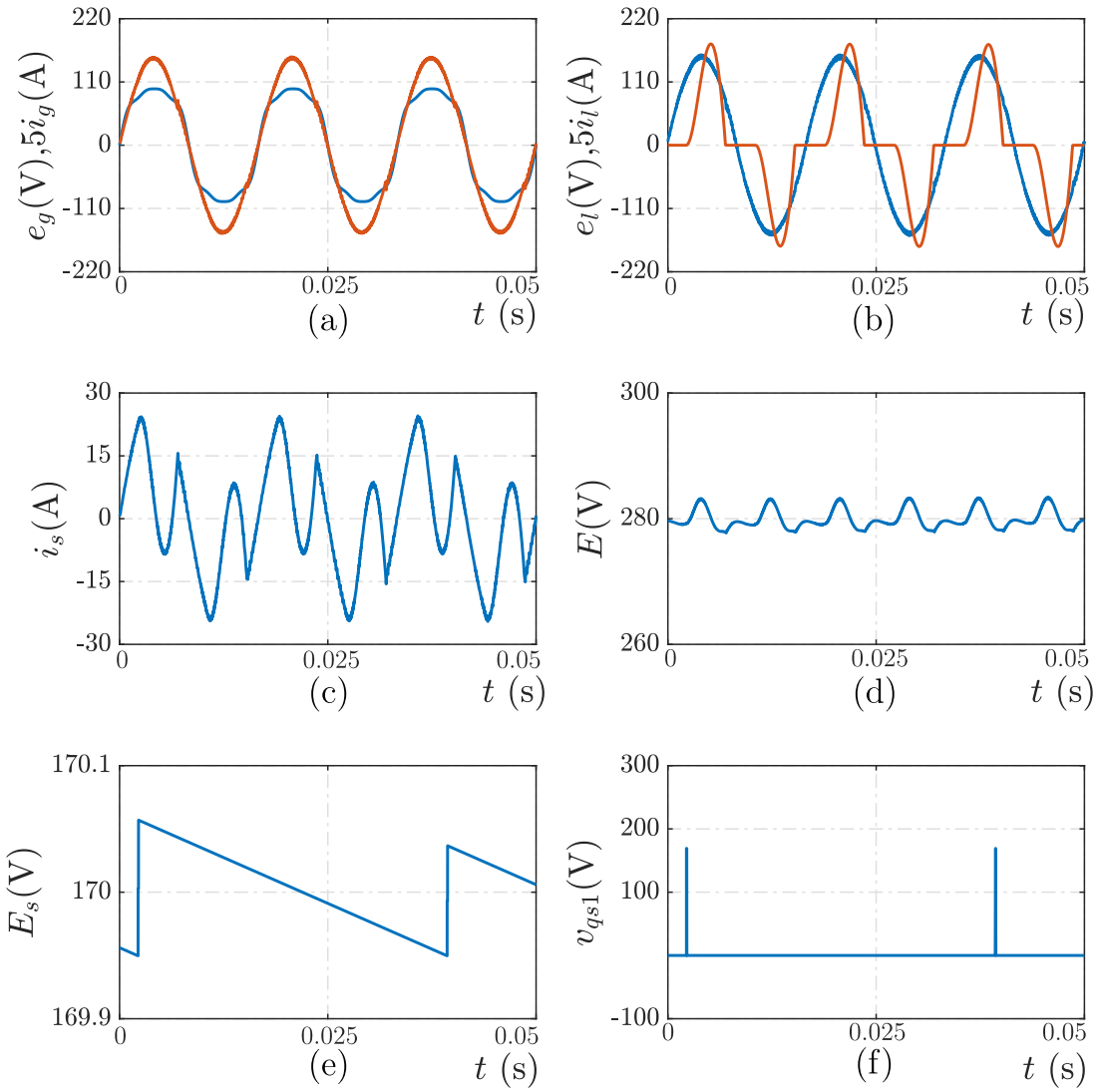


Figure 4.24 – Simulation results of the proposed converter under 30% of grid voltage swell. (a) Grid voltage with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic and grid current. (b) Load voltage and load current. (c) Three-leg module shunt compensation current (i_s). (d) Dc-link voltage of the three-leg module (E). (e) Shunt compensation current (i_h). (f) Dc-link voltage of the shunt module (E_h).

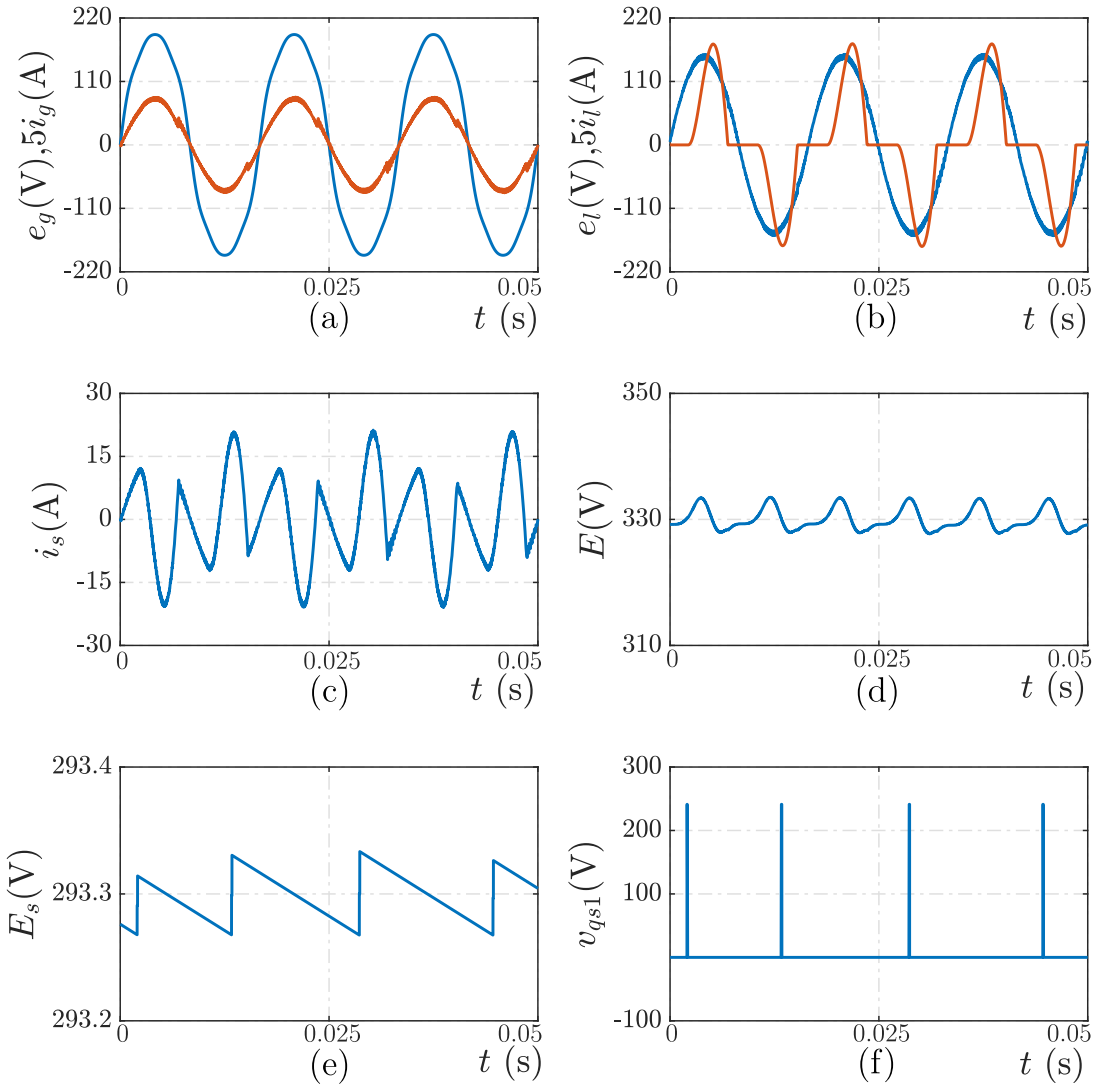


Figure 4.25 – Simulation results with voltage swell transient. Transient caused by a grid voltage swell of 50%.

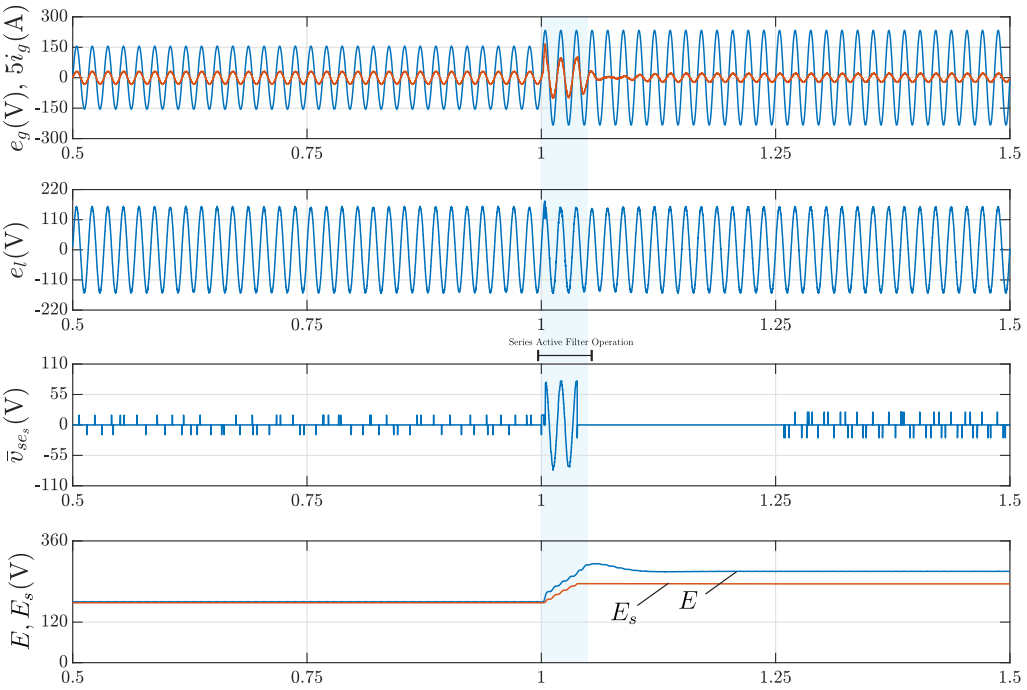


Figure 4.26 – Simulation results with voltage sag transient. Transient caused by a grid voltage sag of 50%.

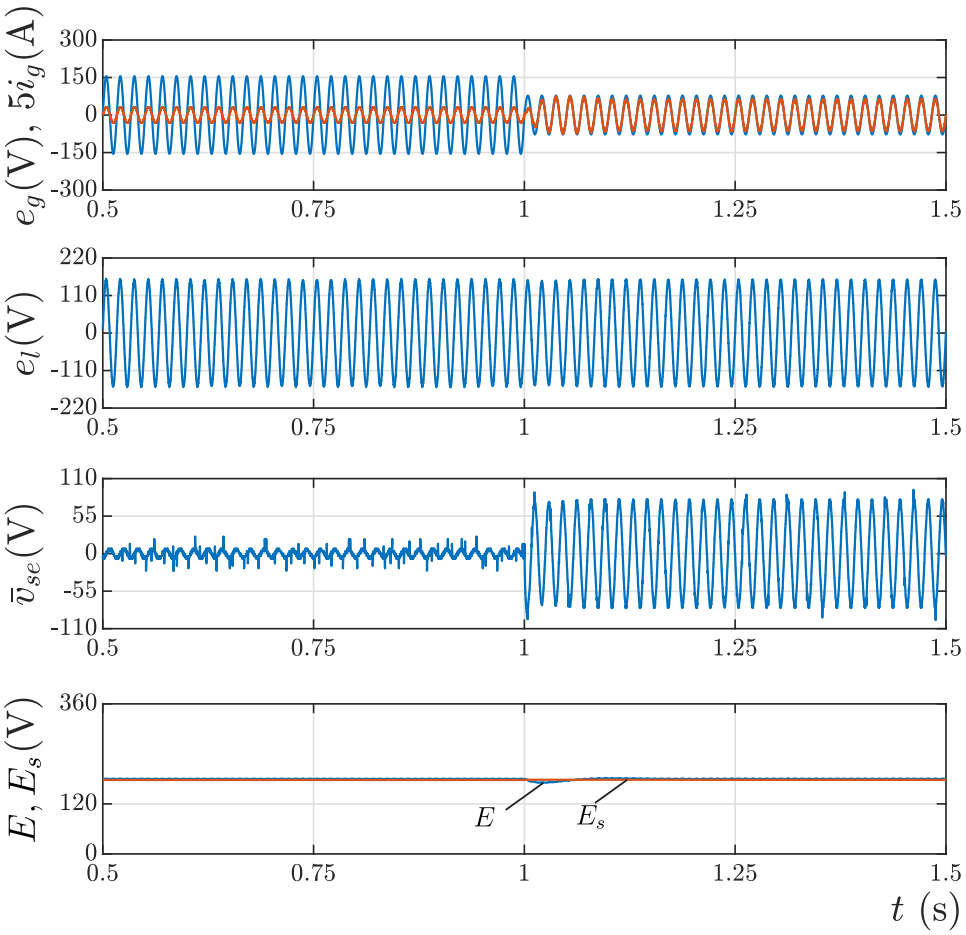
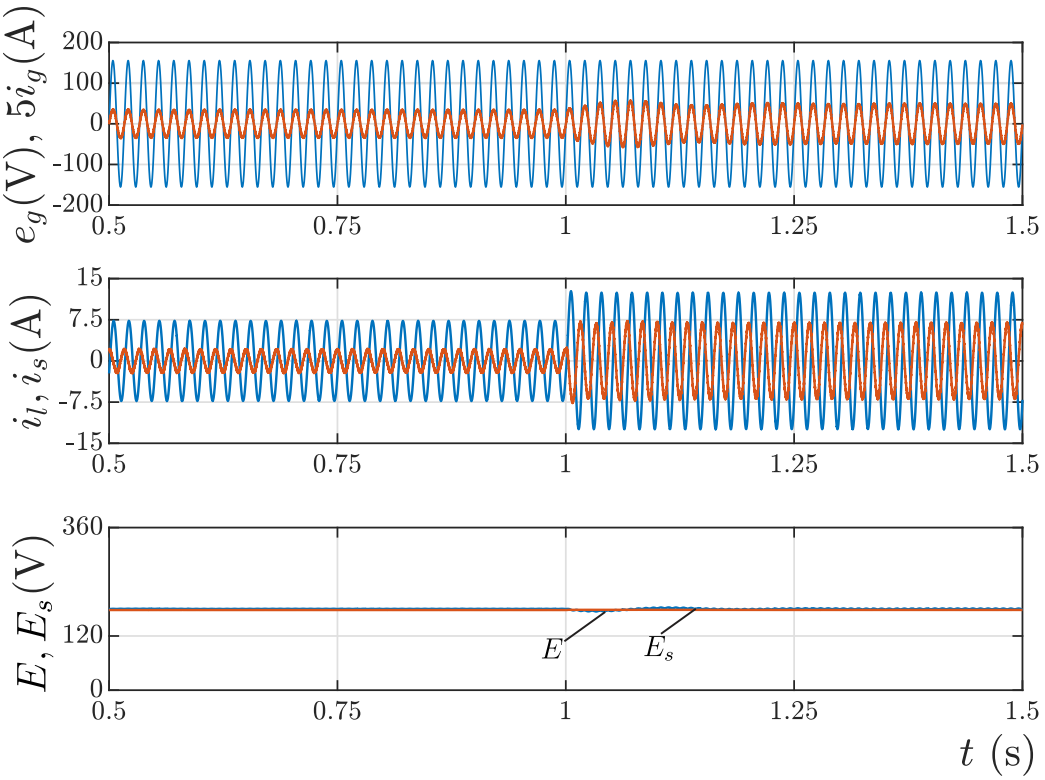


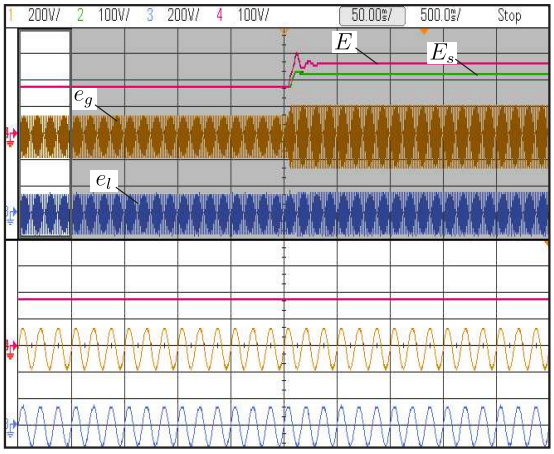
Figure 4.27 – Simulation results with step in the load power. Transient caused by a increase in the load power from $P_l = 536$ W to $P_l = 770$ W.



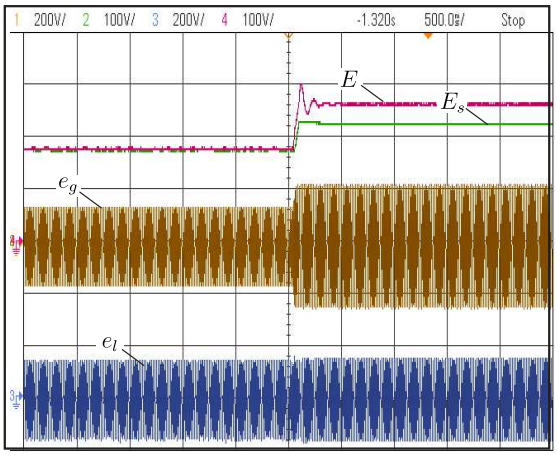
4.4.1.2 Experimental Results

Experimental results were done to confirm the feasibility of the proposed system and the correctness of the design methodology. Figs. 4.28 and 4.29 depict experimental results of a transient caused by a grid voltage swell of 50%. Fig. 4.28(a-c) show the behavior of E, E_s, e_g, and e_l, while Fig. 4.29(a-c) complement with the behavior of i_g and $\bar{v}_{se_s}$. When the disturbance occurs, the two-leg module starts to operate as a series active filter to compensate for the input voltage of the three-leg module (e_l'). Simultaneously, the dc-link reference voltage of the three-leg module (E^*) is changed to deal with the voltage swell. When the voltage E reaches its new reference value, the two-leg module switches back to standby mode. Notice that the load kept compensated. Lastly, Fig. 4.30 presents the behavior of the grid and load voltages and dc-link voltages under a transient caused by a grid voltage sag of 50%. Fig. 4.30(a) depicts the transient in zoom view before the transient, Fig. 4.30(b) shows before and after the transient, and Fig. 4.30(c) presents the transient in zoom view after the transient. One can be seen that the load voltage is compensated and the dc-link voltages regulated.

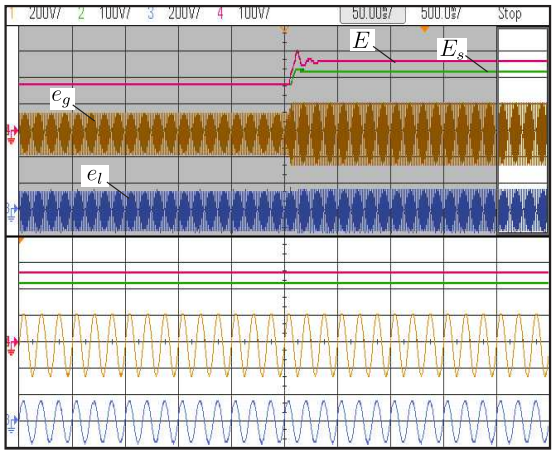
Figure 4.28 – Experimental results with voltage swell transient. Transient caused by a grid voltage swell of 50%. (a) Grid and load voltages (e_g and e_l) and dc-link voltages (E and E_s) with zoom view before the transient. (b) Grid and load voltages (e_g and e_l) and dc-link voltages (E and E_s). (c) Grid and load voltages (e_g and e_l) and dc-link voltages (E and E_s) with zoom view after the transient.



(a)

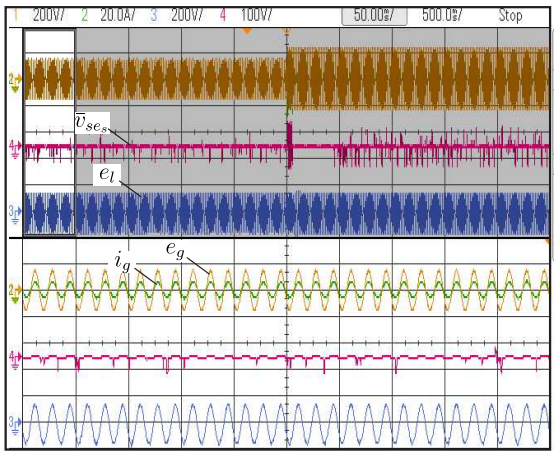


(b)

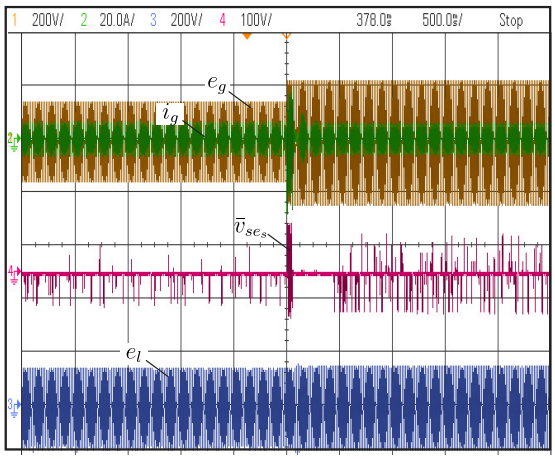


(c)

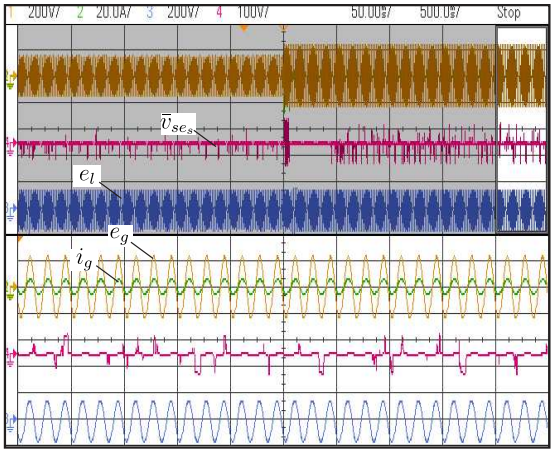
Figure 4.29 – Experimental results with voltage swell transient. Transient caused by a grid voltage swell of 50%. (a) Grid voltage and current (e_g and i_g), series converter voltage of the two-leg module ($\bar{v}_{se_s}$), and load voltage (e_l) with zoom view before the transient. (b) Grid voltage and current (e_g and i_g), series converter voltage of the two-leg module ($\bar{v}_{se_s}$), and load voltage (e_l). (c) Grid voltage and current (e_g and i_g), series converter voltage of the two-leg module ($\bar{v}_{se_s}$), and load voltage (e_l) with zoom view after the transient.



(a)

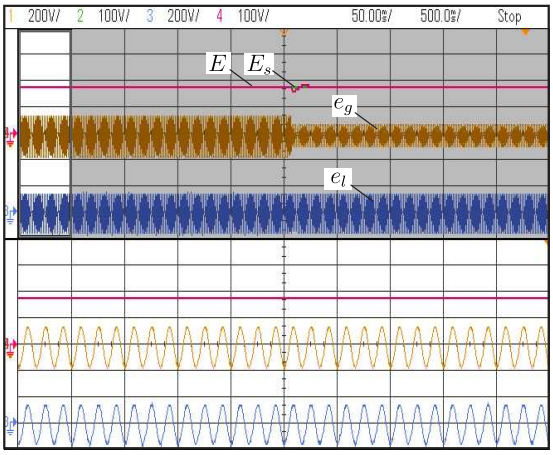


(b)

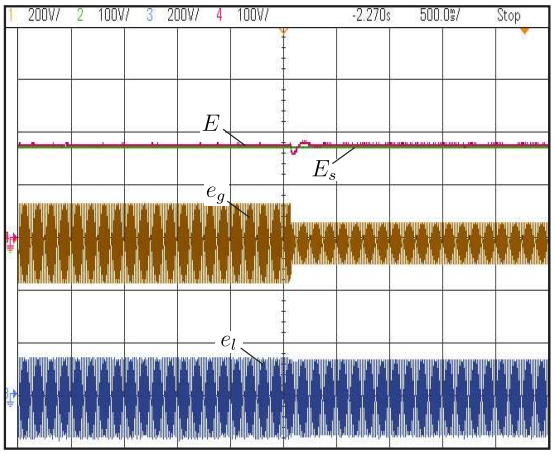


(c)

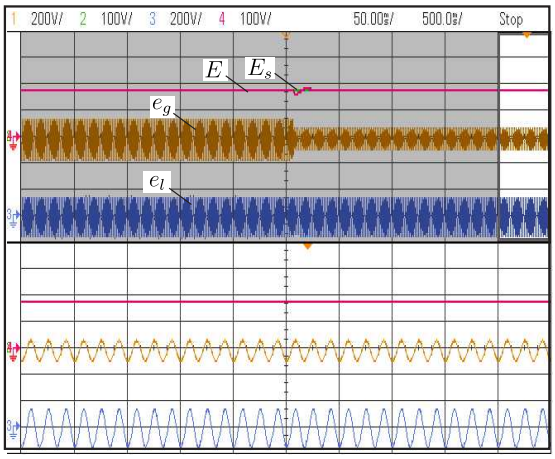
Figure 4.30 – Experimental results with voltage sag transient. Transient caused by a grid voltage sag of 50%. (a) Grid and load voltages (e_g and e_l) and dc-link voltages (E and E_s) with zoom view before the transient. (b) Grid and load voltages (e_g and e_l) and dc-link voltages (E and E_s). (c) Grid and load voltages (e_g and e_l) and dc-link voltages (E and E_s) with zoom view after the transient.



(a)



(b)



(c)

4.5 Five-Leg Converter Based on Three-Leg and Shunt Converters (3LS-SH-UPQC)

This section proposes a transformerless single-phase unified power quality conditioner (UPQC) consisting of a three-leg converter and a hybrid shunt converter. The proposed system provides grid voltage compensation for both sags and swells while simultaneously maintaining a high grid-side power factor with low harmonic content. The system operates with a high modulation index during rated conditions and grid voltage sags. Compared to the conventional single-phase three-leg UPQC, the proposed configuration offers advantages regarding required semiconductor device ratings, harmonic distortion, and power losses. The paper presents the system model, a simplified carrier-based space vector pulse-width modulation scheme, operational constraints, and overall control strategies. Simulation and experimental results are addressed to validate the feasibility of the proposed system.

4.5.1 System Model

Figure 4.31 – Proposed 3LS-SH-UPQC configuration.

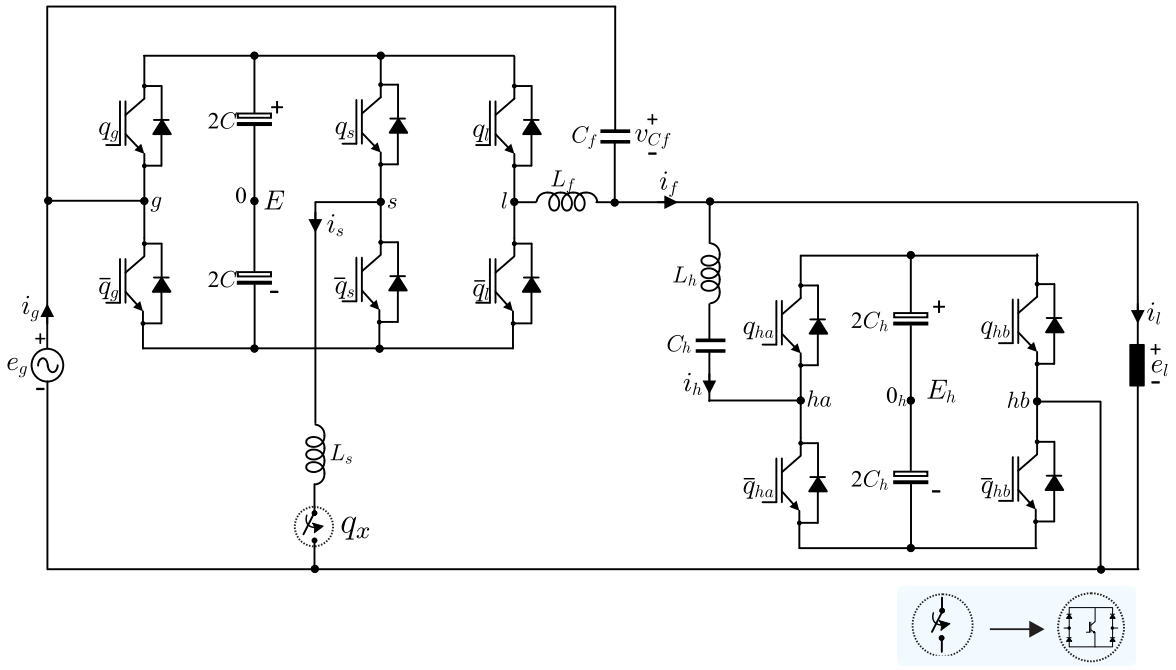
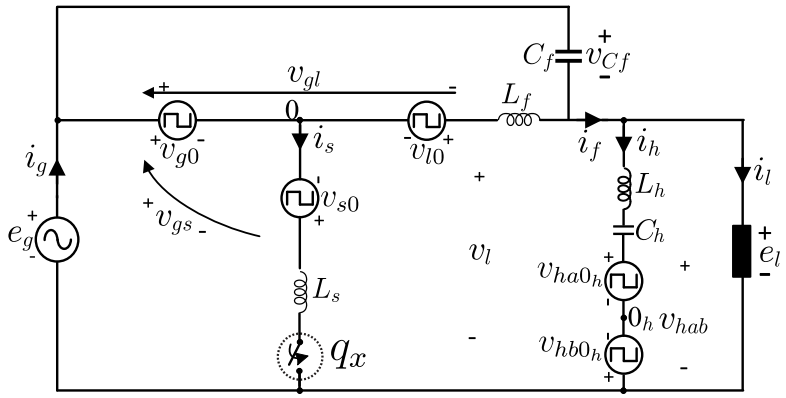


Fig. 4.31 presents the proposed transformerless single-phase UPQC based on three-leg and shunt converters (3L-SH-UPQC). The proposed configuration is composed by a single-phase grid and load voltage (e_g and e_l), a three- and two-leg modules, inductor and capacitor filters (L_s, L_h, C_f, and L_f), two dc links (C, C_h), and a bidirectional switch (q_x) in the leg s. The switches which form the structure are q_j–$\bar{q}_j$ and q_{hn}-$\bar{q}_{hn}$, with $j = \{g, l, s\}$ and $n = \{a, b\}$. Fig. 4.32 presents the equivalent circuit of the studied topology, where

Figure 4.32 – Equivalent circuit.



i_g, i_s, i_f, i_h, and i_l are the grid current, three-leg module shunt compensation current, three-leg module output current, shunt compensation current of the two-leg module, and load current, respectively. The voltages v_{gs} and v_{gl} are the shunt and series converter voltages of the three-leg converter, respectively, and v_{hab} is the output voltage of the shunt converter. The series filter voltage is defined as v_{Cf}. According to Kirchhoff's voltage law and considering that q_x is closed, the voltage loops for both the three-leg [(4.37)-(4.40)] and shunt [(4.41)] converters are defined by

$$v_{gs} = v_{g0} - v_{s0}, \tag{4.37}$$

$$v_{gl} = v_{g0} - v_{l0}, \tag{4.38}$$

$$v_l = e_g - v_{gl}, \tag{4.39}$$

$$v_{Cf} = e_g - e_l, \tag{4.40}$$

$$v_{hab} = v_{ha0_h} - v_{hb0_h}. \tag{4.41}$$

The voltages v_{j0} and v_{hn0_h} are the pole voltages of the three-leg and shunt converters, which are defined as $v_{j0} = (2q_j - 1)E/2$ and $v_{hn0_h} = (2q_{hn} - 1)E_h/2$. E and E_h are the dc-link voltages of the three-leg and shunt converters, respectively. Considering that q_x is opened, the load voltage (e_l) is defined by (4.39).

4.5.2 Dc-link Voltage Requeriments

As already mentioned, the dc-link voltage required for the three-leg converter depends on the amplitude of the voltages of the series and shunt converters. On the series

side, the voltage required to generate the load voltage correctly takes into account the range of the grid voltage sag or swell the converter is designed, while the shunt unit requires sufficient voltage to ensure proper grid current control, which is defined by

$$V_{gs} = E_g - I_s(R_s + jX_s) \tag{4.42}$$

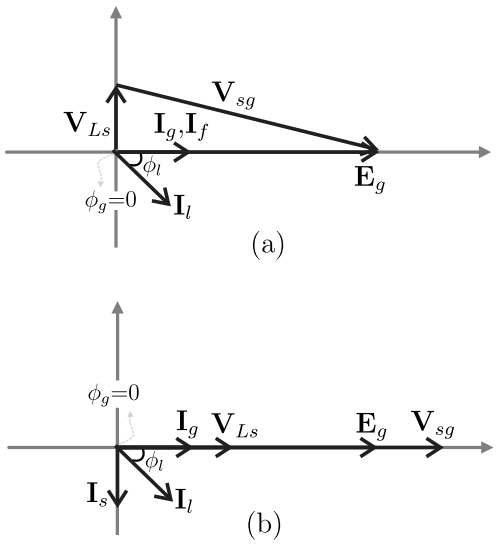
In this way, one can define the following relationship that must be respected:

$$E \geq |E_g - I_s(R_s + jX_s)| \tag{4.43}$$

where R_s denotes the intrinsic resistance of the inductor L_s, and X_s represents its reactance. From (4.43), one can see that the dc-link voltage of the three-leg converter is influenced not only by the grid voltage value, but also by the shunt compensation current, indicating a dependence on the load characteristics.

Fig. 4.33 presents the phasor diagram in rated conditions considering an inductive load for the proposed 3L-SH-UPQC [Fig. 4.33(a)] and 3LS-UPQC [Fig. 4.33(b)] configurations. As expected, in both cases, the shunt converter voltage v_{gs} depends on the three-leg module shunt compensation current i_s, which should be related to the load power factor ($i_s = i_g - i_l$). However, in the proposed system, the shunt hybrid converter handles both harmonic and reactive currents from the load. Therefore, the current i_s is defined only as a portion needed to compensate losses and regulate the dc-link voltage. This allows minimizing i_s and preventing the increase of v_{gs} due to the load power factor variations. Now, considering only a three-leg module, one can note from the phasor diagram presented in Fig. 4.33(b) that the load power factor variations effectively influence in v_{gs}, since the shunt compensation current is composed of reactive current (see Fig. 4.3).

Figure 4.33 – Phasor diagram in rated conditions. (a) For the proposed 3L-SH-UPQC. (b) For 3L-UPQC or 3LS-UPQC.



4.5.3 Hybrid Shunt Converter

To compensate for the additional shunt module in the proposed system, a hybrid filter featuring a series-connected capacitor is employed. This arrangement reduces the power processed by the structure, consequently improving cost and efficiency for a wide range of linear and nonlinear loads (SRIANTHUMRONG; AKAGI, 2003; YıLMAZ; DURNA; ERMIS, 2016). This paper considers in some of the simulation and experimental tests a load with $\cos(\delta_l) = 0.687$ lagging, $e_l = 110$ V, and $S_l = 1.1$ kVA. Taking into account the conventional shunt converter without the series-capacitor, the volt-ampere rating required for the h-bridge converter is

$$S_{shunt} = I_h \cdot V_{hab} \tag{4.44}$$

$$= 7.2650 \cdot 123.6942 = 898.63\text{VA} \tag{4.45}$$

Now, considering for hybrid shunt filter,

$$S_{shunt} = I_h \cdot V_{hab} \tag{4.46}$$

$$= 7.2650 \cdot 51.2465 = 372.30 \text{ VA} \tag{4.47}$$

It can be observed that the series-connected capacitor reduces the processed power by the shunt converter by approximately 58%. This approach, as discussed in subsequent sections, should improve the converter's performance in terms of losses. To define the dc-link voltage value required for generating v_{hab} correctly in the hybrid shunt converter, the following equation can be considered:

$$E_h \geq |V_l - I_h[(R_h + j(X_h - X_c)]| \tag{4.48}$$

where R_h denotes the intrinsic resistance of the inductor, $X_h = \omega L_h$, and $X_c = 1/\omega C_h$.

4.5.4 PWM Strategy

In the proposed system, three-leg and shunt converters are decoupled. In this way, the PWM strategies are analyzed separately. Here, it is propose that the three-leg module is responsible for the series compensation (harmonics, sags and swell in the grid voltage) and the shunt unit for the shunt compensation (harmonics and reactive in the load current).

4.5.4.1 Three-leg Module

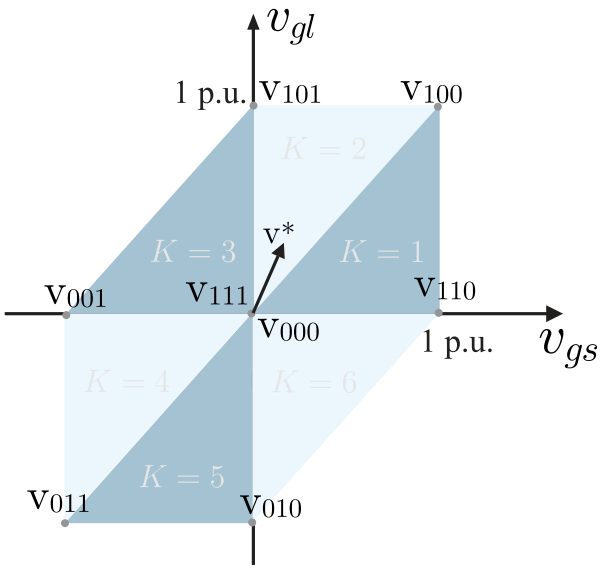
For the three-leg converter, the operation mode depends on the state of the bidirectional switch q_x, either opened or closed. As already mentioned, three-leg converters

based on shared-leg have constraints in scenarios with grid voltage swell, since the converter needs to be designed to operate with a higher dc-link voltage even under rated conditions and grid voltage sags. In this way, the switch q_x in the proposed system, can be used to reconfigure the three-leg converter to a two-leg converter at the onset of a grid voltage swell transient, as presented in section 4.2.4. This reconfiguration ensures uninterrupted operation with a low modulation index under nominal conditions and grid voltage sags.

- **Ac-dc-ac Operation**

To control the three-leg converter, a space-vector pulse-width modulation (SV-PWM) based on carrier-based PWM is employed. In Fig. 4.34, the space-vector plane associated with the three-leg module of the proposed system is illustrated. Each vertex on this plane corresponds to a voltage vector, and the triangles delineate sectors ($K = I, II, III, IV, V, VI$). In this space-vector plane, the voltage vector is defined by $\mathbf{v}_{k_x k_y k_z}$, where k_x, k_y, and k_z are the binary sequences $\{q_g, q_l, q_s\}$ converted to decimal numbers.

Figure 4.34 – Space-vector plane for the three-leg module.



Considering the coordinates in the vector plane, a voltage vector is denoted by $\mathbf{v}_{k_x k_y k_z} = v_{sg} + \mathrm{j}v_{lg}$, where v_{sg} and v_{lg} are the real (Re) and imaginary (Im) parts of the vector. In the SV-PWM technique, the reference voltage, $\mathbf{v}^*_{k_x k_y k_z} = v^*_{sg} + \mathrm{j}v^*_{lg}$, is synthesized by the three closest vectors. These vectors are defined as $\mathbf{v}_x$, $\mathbf{v}_y$, and $\mathbf{v}_z$. Considering $\mathbf{v}^*_{k_x k_y k_z}$ constant during a sampling period T, it can be written that

$$\mathbf{v}^*_{k_x k_y k_z} = \tau_x \mathbf{v}_x + \tau_y \mathbf{v}_y + \tau_z \mathbf{v}_z, \tag{4.49}$$

where τ_x, τ_y, and τ_z represent the duty cycles of the vectors $\mathbf{v}_x$, $\mathbf{v}_y$, and $\mathbf{v}_z$, respectively. The duty cycle of each vector can be determined by

$$\begin{bmatrix} \tau_x \\ \tau_y \\ \tau_z \end{bmatrix} = \begin{bmatrix} \mathrm{Re}(\mathbf{v}_x) & \mathrm{Re}(\mathbf{v}_y) & \mathrm{Re}(\mathbf{v}_z) \\ \mathrm{Im}(\mathbf{v}_x) & \mathrm{Im}(\mathbf{v}_y) & \mathrm{Im}(\mathbf{v}_z) \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} v_{sg}^* \\ v_{lg}^* \\ 1 \end{bmatrix}. \tag{4.50}$$

Considering the null redundant vectors ($\mathbf{v}_{111}$ and $\mathbf{v}_{000}$), it is possible choosing a sequence of vectors to reduce the average switching frequency of the converter. Then, a simplified equivalent carrier-based PWM becomes feasible. Since v_{sg}^* and v_{lg}^* are defined by the shunt and series controllers, respectively, the reference pole voltages can be defined as

$$v_{g0}^* - v_{s0}^* = v_{gs}^* \tag{4.51}$$

$$v_{g0}^* - v_{l0}^* = v_{gl}^* \tag{4.52}$$

Considering the sectors $K = I$ and $K = II$, one can see that v_{g0}^* is constant over a switching period. Therefore, v_{l0}^* and v_{s0}^* can be determined by combining 6.17 and 4.52. This approach can be applied to the other sectors. Taking into account the symmetry of the space-vector plane, for $v_{lg}^* \geq 0$ the reference pole voltages can be calculated as follows

$$\text{if } K = I \text{ or } II,\ v_{g0}^* = -\frac{E^*}{2}, v_{s0}^* = v_{sg}^* - \frac{E^*}{2}, v_{l0}^* = v_{lg}^* - \frac{E^*}{2} \tag{4.53}$$

$$\text{if } K = III,\ v_{l0}^* = \frac{E^*}{2}, v_{g0}^* = -v_{lg}^* + \frac{E^*}{2}, v_{s0}^* = v_{sg}^* - v_{lg}^* + \frac{E^*}{2} \tag{4.54}$$

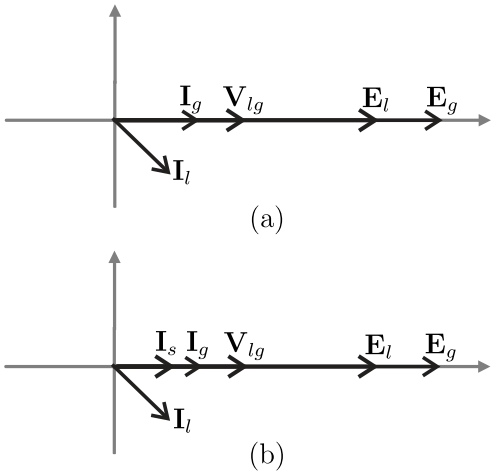
Once calculated the reference pole voltages, the gate command signals of the switches are defined applying a normalized carrier-based PWM technique.

- **H-bridge Operation**

In the proposed three-leg converter, q_x in the leg s allows switching the three-leg converter to a two-leg converter under voltage swells. Considering a monitored grid voltage, upon detection of such an event, the switch q_x is opened and the converter operates as an h-bridge converter until the dc-link voltage surpasses the updated grid voltage amplitude value. Once this condition is met, the switch q_x is closed, restoring the operation as an ac-dc-ac converter and maintaining the swell compensation feature. During the voltage swell increase, the dc-link voltage value is measured and the modulation index of the series converter voltage is updated in each switching period to ensure load voltage compensation.

Since the series converter voltage can be defined when the three-leg cell operates as an h-bridge converter, one can write $v^*_{gl} = v^*_{g0} - v^*_{l0}$. Considering $|v^*_{g0}| \leq 0.5$ p.u. and $|v^*_{l0}| \leq 0.5$ p.u. (with $E = 1$ p.u.), the load voltage remains compensated during the disturbance if the voltage swell is limited to 2 p.u.. In the same way, the switching states of legs g and l are defined by applying a carrier-based PWM. Fig. 4.35 depicts the phasor diagram for the h-bridge and ac-dc-ac operation during a grid voltage swell. Note that the proposed system maintains load voltage compensation and achieves power factor correction throughout the event. It is worth noting that the 3LS-UPQC cannot compensate for the harmonics and reactive currents of the load during the onset of voltage swells because it works as a series h-bridge converter.

Figure 4.35 – Phasor Diagram of 3L-SH-UPQC under voltage swell transient. (a) Phasor diagram at the onset of a grid voltage swell transient (switch q_x is opened). (b) Phasor diagram after the dc-link voltage E has surpassed the grid voltage amplitude value under swell (switch q_x is closed).



4.5.4.2 Shunt Module

The switching states for the shunt hybrid converter are also defined using a carrier-based PWM technique. Taking into account that the reference converter voltage of the shunt hybrid converter is given by the control system, one can define $v^*_{ha0_h}$ and $v^*_{hb0_h}$, respectively as

$$v^*_{ha0_h} = \begin{cases} \frac{E_h}{2}^*, & \text{if } v^*_{hab} \geq 0 \\ -\frac{E_h}{2}^*, & \text{otherwise,} \end{cases} \tag{4.55}$$

$$v^*_{hb0_h} = \begin{cases} \frac{E_h}{2}^* - v^*_{hab}, & \text{if } v^*_{hab} \geq 0 \\ -\frac{E_h}{2}^* - v^*_{hab}, & \text{otherwise.} \end{cases} \tag{4.56}$$

4.5.5 Control System

Fig. 4.36(a) presents the control diagram of the proposed configuration. In this system, the series and shunt controls operate independently. The three-leg converter is in charge of supplying the load with a sinusoidal waveform with the same frequency of the grid, while the shunt converter ensures a high power factor and low harmonic content on the grid side.

The average dc-link voltage value of the three-leg converter (E) is regulated by a conventional PI controller. This block can be used to determine the amplitude of the reference grid current (I_g^*) or the reference shared-leg current (I_s^*). The grid voltage angle (δ_g) is obtained by a single-phase phase-locked loop (PLL). Therefore, it is possible to synchronize i_g with e_g or i_s with e_g, which allows extracting the portion of the active power needed to control the dc-link voltage. To define the shunt converter reference voltage v_{gs}^*, a proportional resonant controller (PR) was implemented.

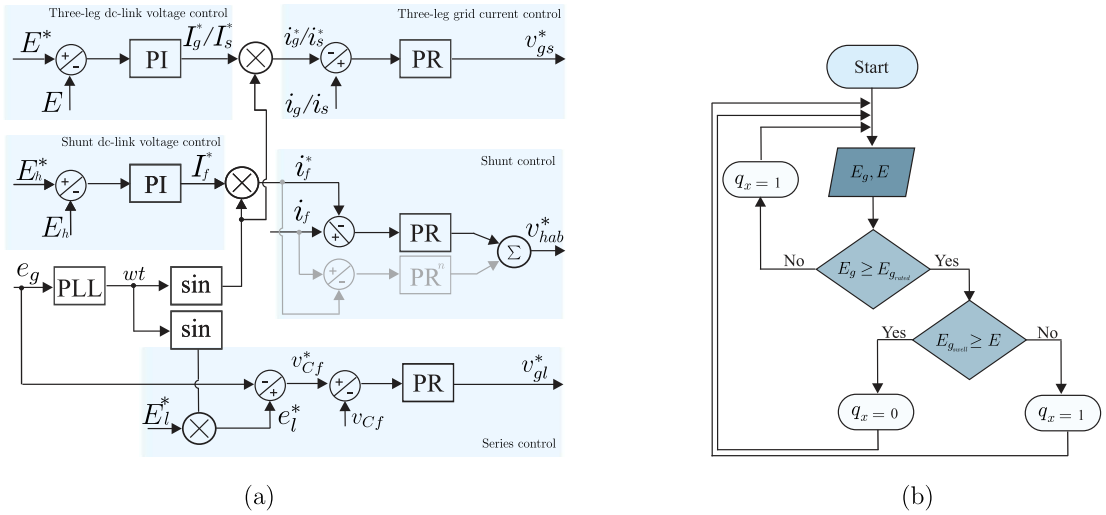
The load voltage control adapts to two operation modes: A) in rated conditions or with voltage sags, and B) voltage swell. In the first mode, the bidirectional switch q_x is closed ($q_x = 1$) and the converter operates as an ac-dc-ac system. This configuration follows the closed-circuit path: e_g - v_{Cf} - $e_l = 0$. In this way, the reference voltage v_{Cf}^* is calculated for a grid voltage and a reference load voltage defined. The controller PR, also a proportional resonant controller, provides the series converter reference voltage v_{lg}^* to control the load voltage. The second operation mode, is considered when the three-leg cell acts as an h-bridge converter ($q_x = 0$). In this moment, the dc-link voltage value is measured and the modulation index of the series converter voltage is updated in each switching period to ensure load voltage compensation. Here, the load voltage control follows the same path: e_g - v_{Cf} - $e_l = 0$. Figure 4.36(b) presents a flowchart illustrating the operation of the bidirectional switch q_x based on grid voltage monitoring.

Similarly, a conventional PI controls the dc-link voltage of the shunt converter (E_h) and produces the amplitude I_f^*. The previously mentioned PLL synchronizes i_f with e_g to minimize the current i_s. The PR block receives the error i_f-i_f^* and provides the output reference voltage of the shunt converter v_{hab}^*. This loop control solves reactive currents from the load. If the load includes harmonic currents, additional PR blocks need to be implemented for each harmonic or at least for the lowest frequency harmonics. Each PR^n block receives the relevant error signal and returns the reference voltage for its respective harmonic.

4.5.6 Results

This section presents simulation and experimental results demonstrating the feasibility of the proposed 3L-SH-UPQC system under closed-loop control. For the experimental tests, power devices from Semikron were used, including IGBTs SKM50GB123D and drivers

Figure 4.36 – Control system. (a) Control diagram to generate the shunt and series reference voltages. (b) Flowchat of the q_x operation.



(a) (b)

SKH23. Additionally, a TMS320F28335 digital signal processor from Texas Instruments controlled the converter

4.5.6.1 Simulation Results

Simulations tests to validate the operation of the proposed structure as a UPQC system were worked out. Unless made clear otherwise, the parameters used in these tests are presented in Table 4.4.

Firstly, the operation of the proposed converter was verified considering grid voltage and load current disturbances simultaneously. In the grid voltage, it was considered harmonics of third (10%), fifth (5%), and seventh (2%) order. For the load, the converter fed a nonlinear load with approximately 70% of harmonic distortion and 1.9 kVA (Nonlinear load I). Figs. 4.37, 4.38, and 4.39 differ from each other by operation, respectively, with the grid voltage under rated conditions, 30% of voltage sag, and 30% of voltage swell, respectively. Notice that the converter ensures grid power factor control, load voltage compensation, and dc-link voltages regulation in the three scenarios. In addition, it is important to highlight that the grid current achieved a THD less than 5% in the three scenarios analyzed.

Next, the simulation results are presented in Figures 4.40, 4.41, and 4.42 to demonstrate the proposed system's capability to compensate for transients such as harmonic and reactive load currents, as well as voltage sags and swells in the grid. The parameters considered for these tests are presented in Table 4.4 (RL load and Nonlinear load II). The proposed converter's capability to compensate for grid voltage disturbances was validated by applying 30% voltage sags and swells. In both cases, it was considered a 1.1 kVA linear load with power factor of 0.68 lagging. Figure 4.40 illustrates the behavior of the three-leg module's dc-link voltage (E) during a voltage swell. The h-bridge operation

begins when the grid voltage exceeds its rated value (t = 2.0). At this point, switch q_x opens, and the dc-link voltage E increases until it exceeds the grid voltage amplitude. Subsequently, q_x closes (approximately t = 2.12), enabling ac-dc-ac converter operation with a new dc-link voltage operating point. Fig. 4.41 shows the operation under a 30% voltage sag. It can be noticed that the proposed system effectively maintains grid power factor correction and load voltage compensation throughout both scenarios. It is important to highlight that the DC-link voltage of the hybrid shunt converter operates at half the value of the dc-link voltage of the three-leg converter. The effectiveness of the grid current and dc-link voltage controls for both the three-leg and shunt modules was validated under a transient where the load power increased by approximately 25%. In this test, it was used a nonlinear load with a harmonic distortion of approximately 40%. As shown in Fig. 4.42, the dc-link voltages remain regulated at their steady-state values, indicating stable operation. Additionally, the grid voltage and current are in phase, ensuring unity grid power factor. Notice that the dc-link voltage of the hybrid shunt converter increased to 130 V, since it was considered the same series-capacitor value designed for the previously test. However, the LC filter can also be designed for a specific harmonic allowing a reduction in the dc-link voltage.

Table 4.4 – Parameters used in simulations and experimental tests.

Parameter		Value
Grid voltage	e_g	110 V rms 77 V rms 143 V rms
Load reference voltage	e_l^*	110 V rms
Switching frequency	f_s	10 kHz
Dc-link capacitor	C	2.2 mF
Three-leg shunt inductance	L_s	5 mH
Hybrid shunt inductance	L_h	5 mH
Hybrid shunt capacitance	C_h	266 μF
Series filter inductance	L_f	2 mH
Series filter capacitance	C_f	18 μH
Series filter dump resistance	R_f	10 Ω
RL Load		
Dc-link voltage	E, E_h	170/85 V
Load power factor	$\cos(\delta_l)$	0.68 (lagging)
Apparent power	S_l	1.1 kVA
Nonlinear load I		
Dc-link voltage	E, E_h	170/100 V
Apparent power	S_l	1.9 kVA
Load current THD	THD_{il}	70%
Nonlinear load II		
Dc-link voltage	E, E_h	170/130 V
Apparent power	S_l	0.82/1.1 kVA
Load current THD	THD_{il}	40%

Figure 4.37 – Simulation results of the proposed converter under nominal conditions. (a) Grid voltage with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic and grid current. (b) Load voltage and load current. (c) Three-leg module shunt compensation current (i_s). (d) Dc-link voltage of the three-leg module (E). (e) Shunt compensation current (i_h). (f) Dc-link voltage of the shunt module (E_h).

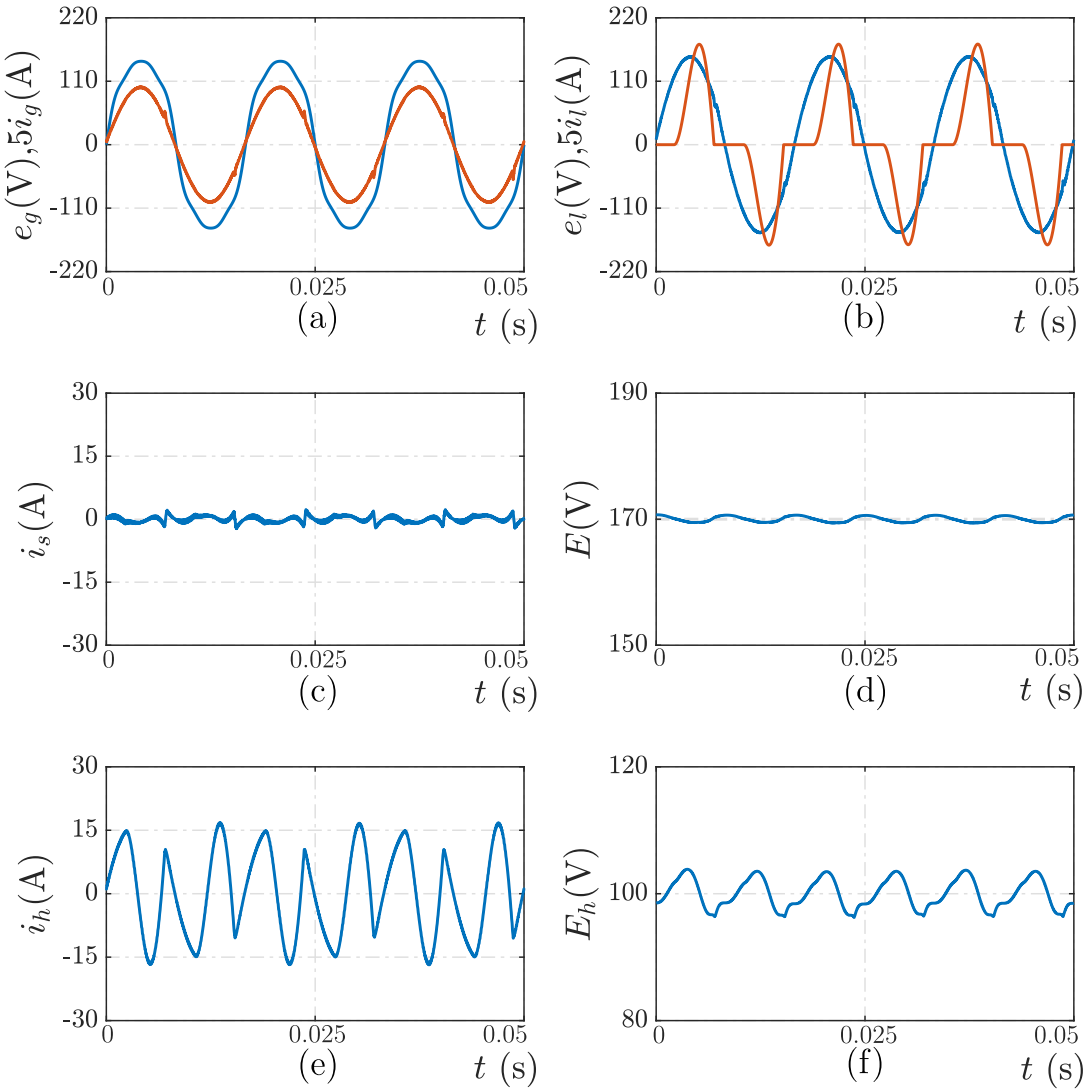


Figure 4.38 – Simulation results of the proposed converter under 30% of grid voltage sag. (a) Grid voltage with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic and grid current. (b) Load voltage and load current. (c) Three-leg module shunt compensation current (i_s). (d) Dc-link voltage of the three-leg module (E). (e) Shunt compensation current (i_h). (f) Dc-link voltage of the shunt module (E_h).

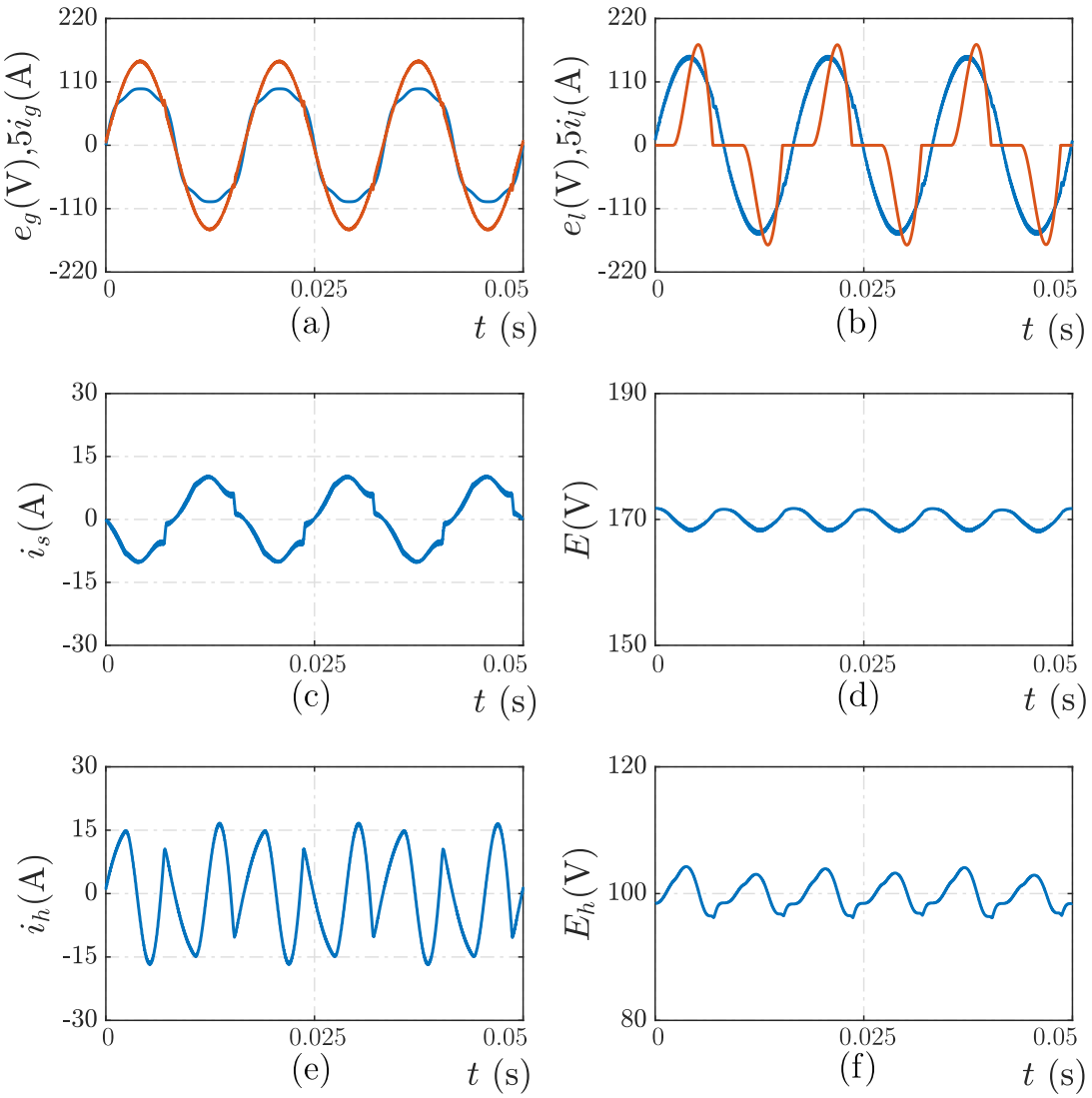


Figure 4.39 – Simulation results of the proposed converter under 30% of grid voltage swell. (a) Grid voltage with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic and grid current. (b) Load voltage and load current. (c) Three-leg module shunt compensation current (i_s). (d) Dc-link voltage of the three-leg module (E). (e) Shunt compensation current (i_h). (f) Dc-link voltage of the shunt module (E_h).

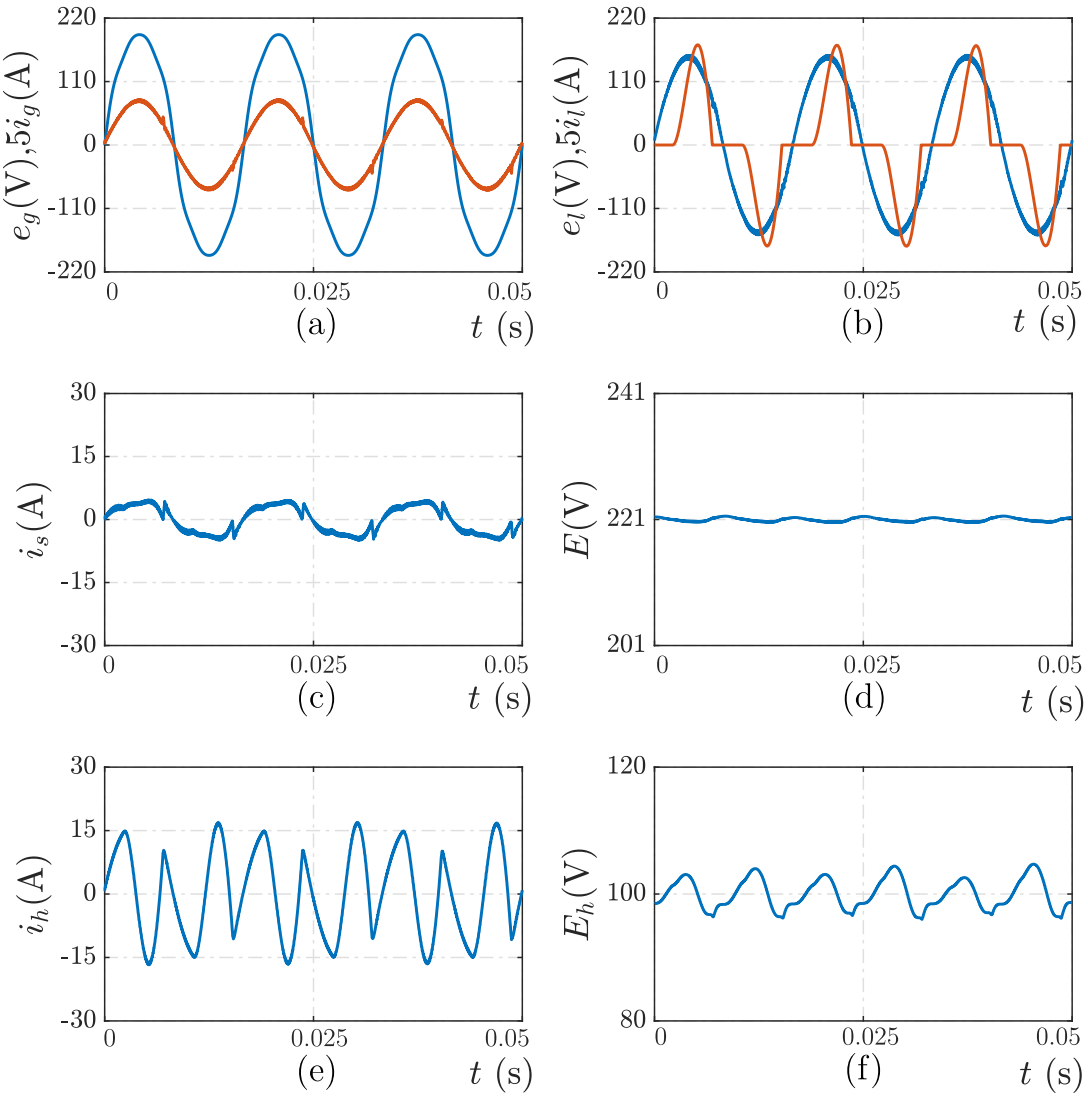


Figure 4.40 – Simulation results of the proposed converter under a voltage swell of 30%.

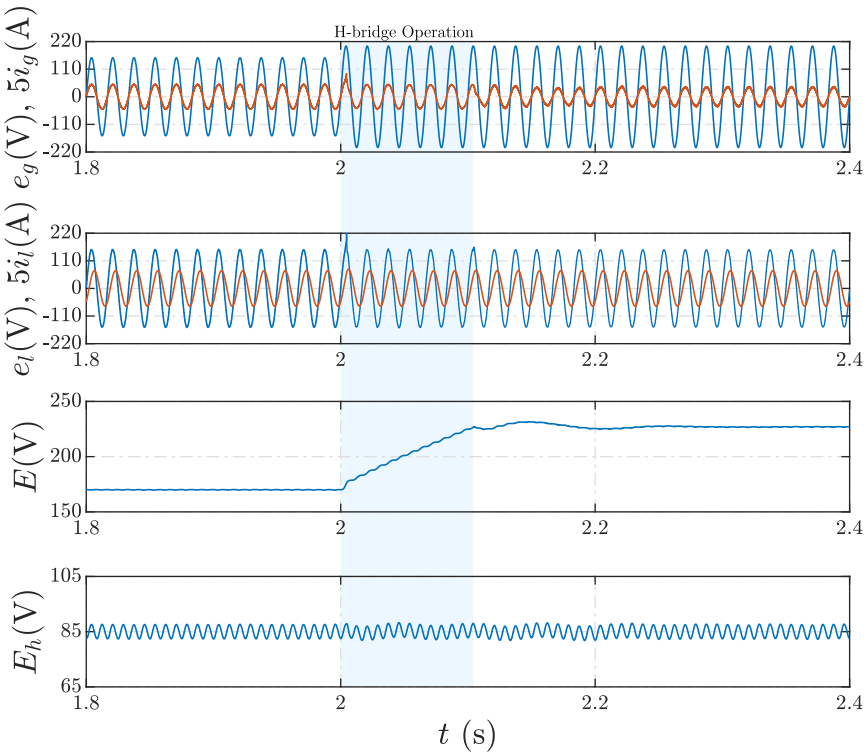


Figure 4.41 – Simulation results of the proposed converter under a voltage sag of 30%.

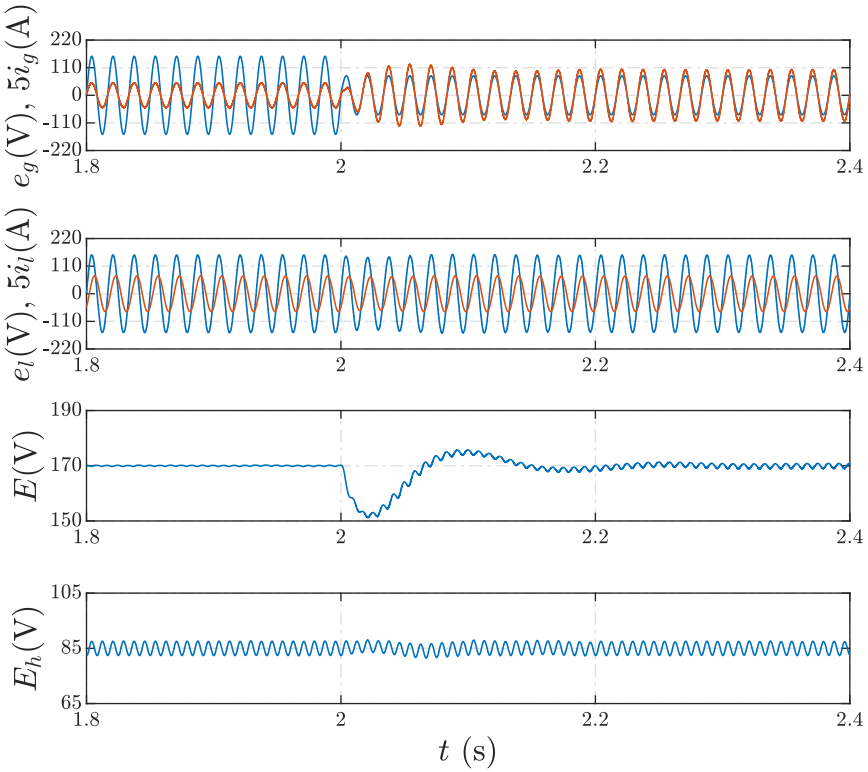
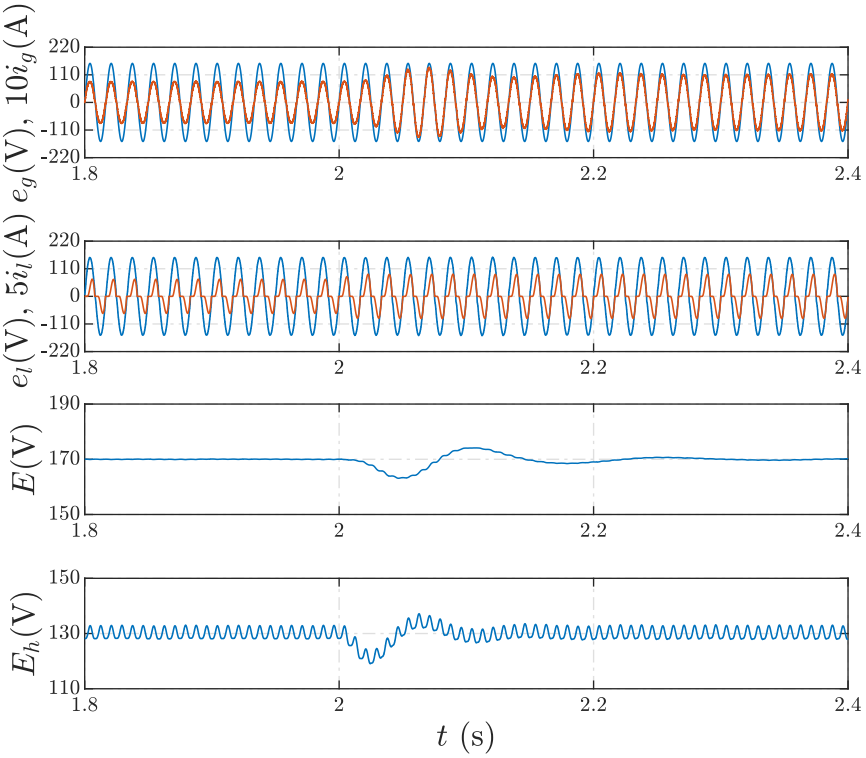


Figure 4.42 – Simulation results of the proposed converter under rated conditions with a step in the load power from $S_l = 0.82$ kVA to $P_l = 1.1$ kVA.

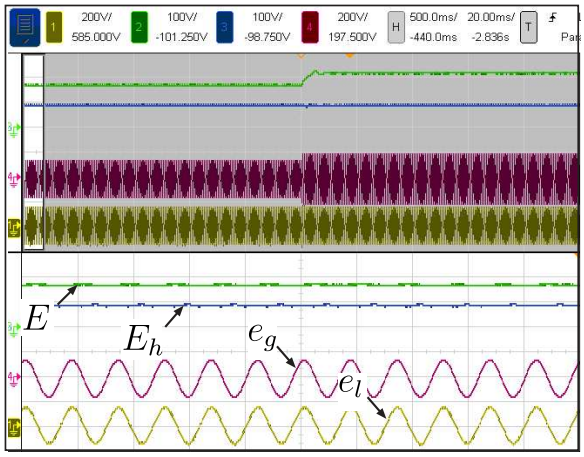


4.5.6.2 Experimental Results

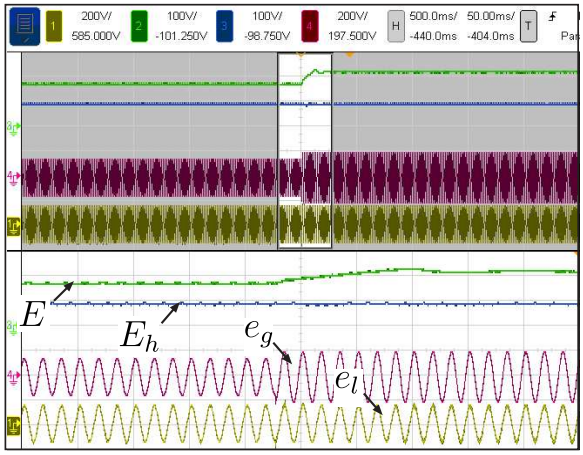
To validate the simulation tests, experimental results were performed for the proposed 3L-SH-UPQC system. Figs 4.43, 4.44, and 4.45 present experimental results for the proposed converter operating under grid voltage disturbances and load step. The parameters used are presented in Table 4.4. For each disturbance, a full view (500 ms/) of the transient and zoomed views (20 ms/) before [see Figs. 4.43(a), 4.44(a), and 4.45(a)], in the beginning [see Figs. 4.43(b), 4.44(b), and 4.45(b)], and during [see Figs. 4.43(c), 4.44(c), and 4.45(c)] the transient is provided. Fig. 4.43 demonstrates the capability of the proposed converter to compensate 30% of voltage swell. At the beginning of the disturbance, switch q_x is opened and the configuration operates as a series h-bridge converter until the dc-link voltage E becomes higher than the amplitude of the grid voltage. The converter then returns to ac-dc-ac operation, maintaining the load voltage compensation throughout the disturbance. It is essential to highlight that after the voltage swell transient, the dc-link voltage should return to the nominal value to ensure high modulation index operation. In addition, during the entire disturbance, the hybrid shunt converter is responsible for ensuring that the grid's power factor remains controlled. Fig. 4.44 illustrates a voltage sag transient of 30%. It can be observed that the dc-link voltages and the load voltage kept controlled. In the experimental swell and sag tests a linear load of 1.1 kVA with a power factor of 0.68 lagging was used. Lastly, Fig. 4.45 presents a transient caused by a load increase of 25%. In this tests it was considered a nonlinear load with harmonic distortion

of, approximately, 38%. As can be seen, the hybrid shunt converter ensured grid power factor correction before and after the transient. The increase in the load current generate an increase in the grid current to adjust the dc-link voltages.

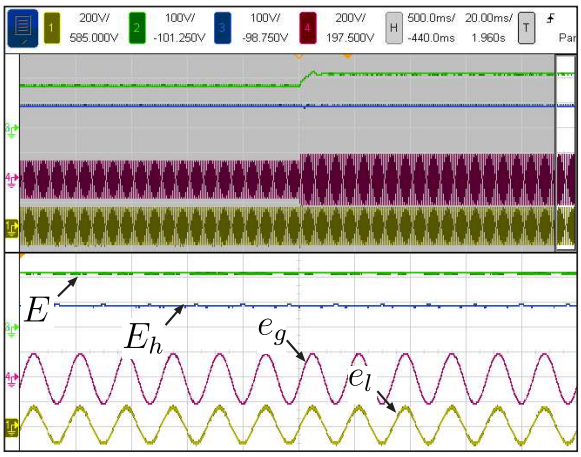
Figure 4.43 – Experimental results - Grid voltage swell of 30%. Grid (e_g) and load (e_l) voltages and dc-link voltages (E and E_h) with zoomed view (a) before of the disturbance, (b) in the beginning of the disturbance, and (c) during the disturbance.



(a)

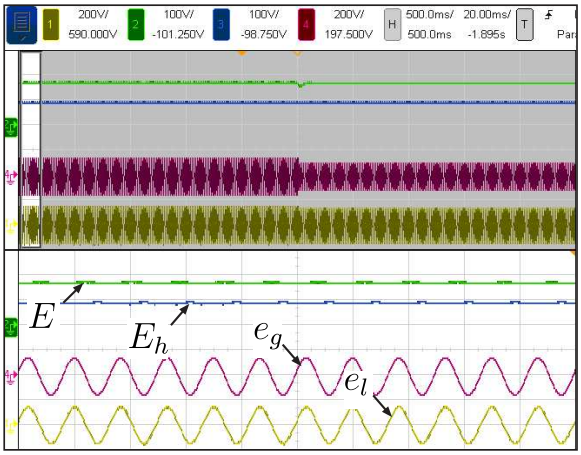


(b)

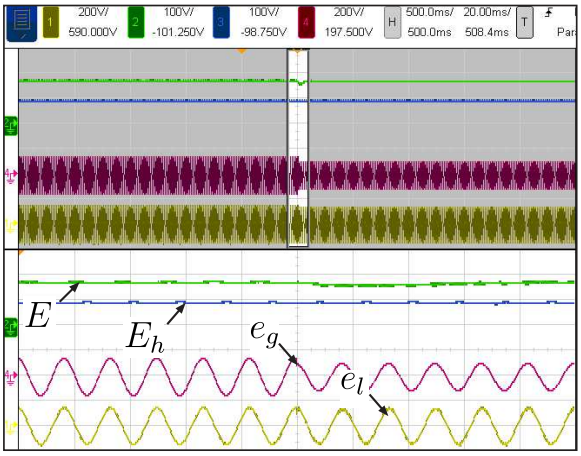


(c)

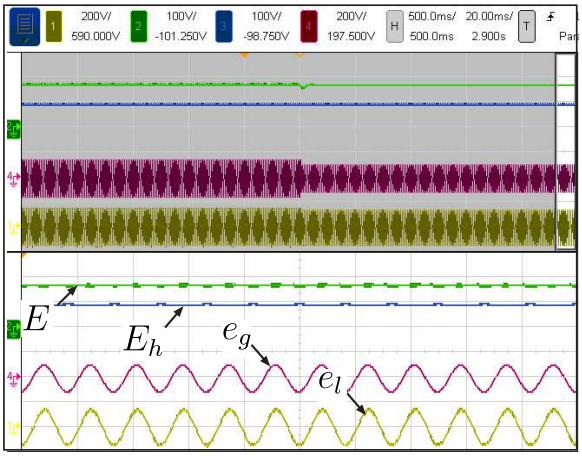
Figure 4.44 – Experimental results - Grid voltage sag of 30%. Grid (e_g) and load (e_l) voltages and dc-link voltages (E and E_h) with zoomed view (a) before of the disturbance, (b) in the beginning of the disturbance, and (c) during the disturbance.



(a)

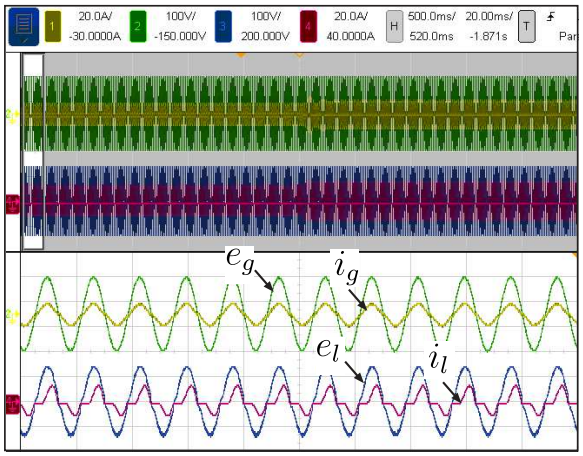


(b)

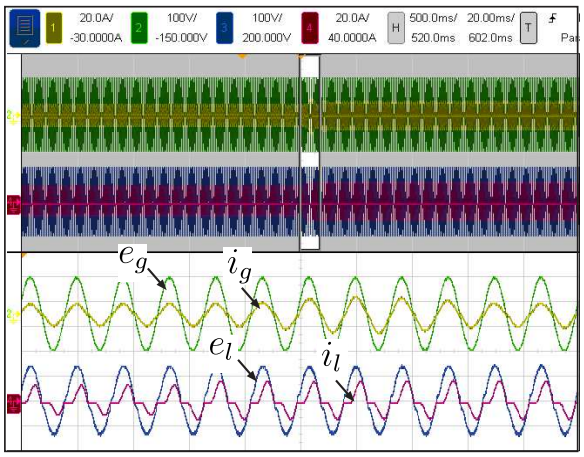


(c)

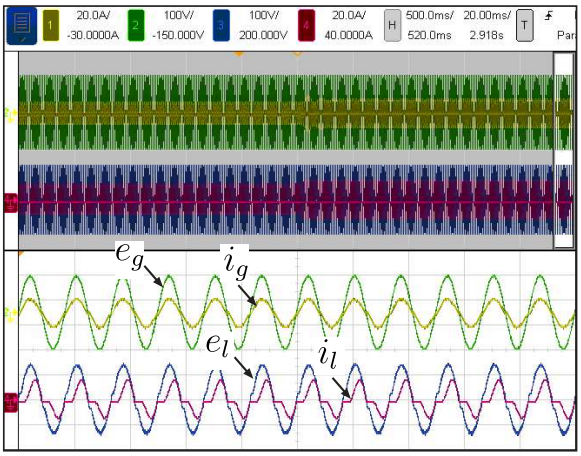
Figure 4.45 – Experimental results - Step in the load power from $S_l = 0.82$ kVA to $S_l = 1.1$ kVA. Load voltage (e_l), grid voltage (e_g), grid current (i_g), and load current (i_l) (a) before the load transient, (b) in the beginning of the load transient, and (c) during the load transient.



(a)



(b)



(c)

4.6 Comparison of the Topologies

In this section, 3L-UPQC, 3LS-UPQC, SB-3L-UPQC, and 3L-SH-UPQC converters are analyzed in terms of blocking voltage on the power switches, harmonic distortion, and power losses. The tests have been performed in closed-loop control and the parameters presented in Table 4.5 were considered. The analysis related to harmonic distortion and power losses considers three cases:

- Case A - Rated condition;
- Case B - 50% grid voltage swell;
- Case C - 50% grid voltage sag.

Table 4.5 – Parameters considered for the tests.

Parameter		Value
Rated load power	P_l	1 kW
Load power factor	$\cos(\delta_l)$	0.7 lagging
Reference load voltage amplitude	E_l^*	155.6 V
Grid voltage amplitude	E_g	155.6 V
Dc-link voltage - 3L-SH-UPQC	E, E_h	170/75 V
Dc-link voltage - 3L-UPQC	E	392 V
Dc-link voltage - 3LS-UPQC	E	196 V
Dc-link voltage - SB-3LS-UPQC	E, E_s	196/170 V
Switching frequency	f_s	10 kHz
Grid and load frequency	f_g/f_l	60/60 Hz
Three-leg shunt inductance	L_s	5 mH
Hybrid shunt inductance	L_h	5 mH
Hybrid shunt capacitance	C_h	300 μF
Series filter inductance	L_f	2 mH
Series filter capacitance	C_f	18 μH
Series filter dump resistance	R_f	10 Ω
Dc-link capacitor	C	2.2 mF

4.6.1 Rating of the Semiconductor Devices

The voltage rating of the power switches is determined by the dc-link voltage. Given that the four investigated converters are designed to compensate for grid voltage swells of up to 1 p.u., the minimum dc-link voltage needed to ensure series compensation under all conditions is 1 p.u.. However, in order to enable simultaneous series and shunt compensation, (4.12) must also be taken into account when designing the dc-link voltage. Table 4.6 presents the blocking voltage on the power switches for the four converters. It becomes evident that the conventional 3L-UPQC converter requires a significantly higher dc-link voltage compared to the 3LS-UPQC and 3L-SH-UPQC, indicating a limitation of this

configuration in maintaining all its UPQC functionalities when designed to handle voltage swells. For the 3LS-UPQC and SB-3LS-UPQC, the dc-link voltage design incorporates the load characteristics, which can become a major disadvantage for loads with low power factors (see Fig. 4.3). In the 3LS-SH-UPQC system, the dc-link voltage of the three-leg converter must just exceed the amplitude of the grid voltage, while the dc-link voltage of the hybrid shunt converter can be calculated using (4.48).

Table 4.6 – Rating of the semiconductor devices.

3L-SH-UPQC					
Switch	q_g	q_l	q_s	q_{ha}	q_{hb}
Voltage (p.u.)	1.09	1.09	1.09	0.48	0.48
3L-UPQC					
Switch	q_g	q_l	q_s		
Voltage (p.u.)	2.51	2.51	2.51		
3LS-UPQC					
Switch	q_g	q_l	q_s		
Voltage (p.u.)	1.26	1.26	1.26		
SB-3LS-UPQC					
Switch	q_g	q_l	q_a	q_{s1}	q_{s2}
Voltage (p.u.)	1.26	1.26	1.26	1.09	1.09

*1 p.u. = 155.6 V

4.6.2 Harmonic Distortion

The total harmonic distortion (THD) of the grid currents (i_g) and load voltage (e_l) have been calculated to compare the investigated configurations. The THD can be calculated by

$$THD(\%) = \frac{100}{\sigma_1}\sqrt{\sum_{n=2}^{N_x}\sigma_n^2} \tag{4.57}$$

where σ_1 is the amplitude of the fundamental component, σ_n is the amplitude of the harmonic of order n, and N_x is the number of harmonics that are used in the calculation. The THD and WTHD were obtained using $N_x = 1000$ components. Table 4.7 presents the THD for the four studied configurations. As expected, because of its high dc-link voltage, 3L-UPQC showed the worst results in all analyzed scenarios, while 3LS-UPQC, 3LS-SH-UPQC, and SB-3LS-UPQC showed similar results.

Table 4.7 – THD analysis.

Case A		
Converter	THD (%)	
	i_g	e_l
3L-SH-UPQC	1.49	1.01
3L-UPQC	3.19	1.79
3LS-UPQC	1.71	1.07
SB-3LS-UPQC	1.84	1.12
Case B		
Converter	THD (%)	
	i_g	e_l
3L-SH-UPQC	4.18	3.16
3L-UPQC	5.01	3.90
3LS-UPQC	4.05	3.29
SB-3LS-UPQC	4.12	3.35
Case C		
Converter	THD (%)	
	i_g	e_l
3L-SH-UPQC	0.90	2.18
3L-UPQC	1.16	4.49
3LS-UPQC	0.95	2.35
SB-3LS-UPQC	1.01	2.39

4.6.3 Power Losses

The power losses of the configurations investigated were calculated using the thermal modules of the PSIM V9.1 software. The IGBT SKM50GB063D from Semikron was used as the power switch in the analysis. The power loss calculations took into account conduction losses (P_{cd}), switching losses (P_{sw}) and the total power losses ($P_t = P_{cd} + P_{sw}$). Table 4.8 shows the power losses for the three scenarios analyzed. As can be seen, the conventional 3L-UPQC presents the worst results for the three scenarios. This is due to the high value of the dc-link voltage, which mainly affects the switching losses of the converter. It can also be observed that the proposed 3LS-SH-UPQC, although it has two additional legs compared to the 3LS-UPQC, has a similar overall power loss. This is achieved due to the low power consumption of the hybrid shunt converter, the minimized three-leg shunt compensation current, and the high modulation index operation. For the SB-3LS-UPQC, it was found that the conduction losses due to the standby converter affect the overall losses of the structure and show the worst results compared to 3LS-UPQC and 3LS-SH-UPQC. It is important to emphasize that the design of the dc-link voltage value of 3L-UPQC, 3LS-UPQC, and SB-3LS-UPQC depends on the load power characteristics, which can lead to operation with a low modulation index, as shown in Fig. 4.3. In this way, the proposed 3LS-SH-UPQC is the most promising of the investigated configurations.

Table 4.8 – Semiconductor power losses.

Case A				
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)	E_f (%)
3L-SH-UPQC	28.7	19.3	48.02	95.2
3L-UPQC (conv.)	24.1	47.3	71.4	92.8
3LS-UPQC	24.6	24.1	48.6	95.1
SB-3LS-UPQC	36.9	24.3	61,2	93.9
Case B				
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)	E_f (%)
3L-SH-UPQC	26.4	25.2	51.6	94.8
3L-UPQC (conv.)	21.7	43.2	64.9	93.5
3LS-UPQC	22.0	30.9	53.0	94.7
SB-3LS-UPQC	28.9	31.3	60.2	94.0
Case C				
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)	E_f (%)
3L-SH-UPQC	49.3	32.5	81.9	91.8
3L-UPQC (conv.)	38.7	70.4	108.8	89.1
3LS-UPQC	42.2	37.7	79.9	92.0
SB-3LS-UPQC	61.6	38.0	99.6	90.0

4.7 Conclusion

In this Chapter, it were proposed three new decoupling methods to improve the performance of the single-phase ac-dc-ac three-leg converter. First, it was proposed a reconfiguration of the three-leg module by using a bidirectional switch to allow decoupling of the series and shunt unit under grid voltage swell. This approach presents issues related to the difficulty of reconfiguration under highly inductive loads. Additionally, during the reconfiguration, the converter can no longer ensure grid power factor correction. To solve these issues, a transformerless single-phase UPQC based on three-leg and standby converters, named here SB-3LS-UPQC, was proposed. The standby operation proposed here aimed a low power consumption of a two-leg module during rated conditions and grid voltage sags. Under grid voltage swells, the two leg module operates as a series active filter to compensate the input side of the three-leg module during the onset of the disturbance, avoiding the use of a bidirectional switch and the operation without grid power factor correction.

Although 3LS-UPQC and SB-3LS-UPQC have addressed the issues related to the operation of the conventional 3L-UPQC configuration with high dc-link voltage even under rated conditions and grid voltage sags, it was verified that problems related to the dependence on the load characteristics in the design of the dc-link voltage, potentially still leading to operation with a low modulation index. In this way, a transformerless single-phase UPQC consisting of a three-leg converter and a hybrid shunt converter (3LS-

SH-UPQC) was proposed. Compared to the conventional three-leg converter, 3LS-UPQC, and SB-3LS-UPQC, the proposed 3LS-SH-UPQC does not present issues related to the dependence on the load characteristics, since the hybrid shunt converter was responsible for compensating the harmonic and reactive power from the load. In addition, employing a series-connected capacitor in the shunt converter allowed operation with low power consumption. As a result, the power losses analysis indicated that, although the proposed 3L-SH-UPQC has more semiconductor devices, it presented better results than 3L-UPQC and similar performance compared to 3LS-UPQC and SB-3LS-UPQC.

Chapter 5

A Transformerless Unified Power Quality Conditioner Based on Four-Leg Converter

With the increasing use of semiconductor-based electronic devices connected to the power grid, power quality issues such as voltage sag and swell, flickers, reactive power, and harmonics have become a significant concern (HEENKENDA et al., 2023). To address these challenges, several single-phase converter topologies operating as unified power quality conditioners (UPQC) have been proposed (KHADKIKAR, 2012). The most well-known UPQC topology for single-phase applications is the full-bridge UPQC [see Fig. 1.2]. This topology consists of two h-bridge voltage source inverters, a line-frequency transformer (LFT), and a dc-link capacitor connecting the series and shunt units.

To avoid the use of LFTs, in (SANTOS et al., 2014), a transformerless single-phase four-leg converter is proposed for size and weight critical applications. This configuration can compensate harmonic and reactive currents, however, issues related to circulating current are also addressed. The open transformerless UPQC (PENG et al., 2016), here called 4L-OPEN-UPQC, should also be emphasized. This converter offers decoupled series and shunt modules similar to the conventional full-bridge. However, its operation without a fixed dc source in the series converter's dc-link presents drawbacks such as the load voltage phase jump and non-unity grid power factor during grid voltage disturbances.

In terms of cost and efficiency, two and three-leg structures are more suitable than four-leg converters, as the number of power switches can be reduced. Concerning these structures, the three-leg converter, stands out in the literature as it reduces the number of power switches compared to a full-bridge UPQC and provides half the reverse voltage to all switches for the same load voltage amplitude compared to a half-bridge converter.

However, assuming that both structures are designed to compensate voltage swell on the grid side, issues related to power losses and harmonic distortion arise when operating with a high dc-link voltage value even under nominal conditions. In addition, the dc-link voltage value depends on the characteristics of the load power, which can even worsen the modulation index. In (CARDOSO; JACOBINA; FELINTO, 2022), a new decoupled method was proposed to improve operation under grid voltage swells without affecting the modulation index at nominal voltage and grid voltage sag. However, this approach raises problems related to the difficulty of reconfiguration with highly inductive loads. In addition, during reconfiguration, the converter can no longer guarantee correction of the grid power factor and operation with regenerative loads. To solve these problems, a single-phase UPQC system based on three-leg and shunt converters was proposed in (CARDOSO et al., 2022), which extends the compensation range under grid voltage swells and nominal conditions compared to an open UPQC and a conventional three-leg converter. For proper operation, however, additional control loops and voltage and current sensors are required, which increase the complexity of the overall control system.

In this chapter, a single-phase transformerless unified power quality conditioner (UPQC) based on two h-bridge modules is proposed. In the proposed configuration, the way the load is connected allows the natural dc-link voltage balancing, which simplifies the design of the control strategy compared to the conventional transformerless UPQCs. The proposed configuration can compensate for grid voltage disturbances and provide grid power factor correction operating with minimum dc-link voltage values. The system model, operating conditions, overall control system, and a pulse width modulation that exploits a simplified carrier-based approach are presented. Simulation and experimental results are also presented to evaluate the feasibility of the proposed system.

5.1 System Model

Fig. 5.1 shows the proposed single-phase four-leg transformerless UPQC, here called 4L-UPQC. The configuration consists of a single-phase grid and load voltage (e_g and e_l), four two-level legs, inductor and capacitor filters (L_{se}, C_{se}, and L_{sh}), and two dc-link capacitors whose voltages are denoted as E_a and E_b. In such a configuration, the legs ha and hb are common between the shunt and series sides of the converters. Fig. 5.2 shows the simplified equivalent circuit of the proposed configuration, where v_{sh} and v_{se} are the shunt converter voltage and series converter voltage, respectively; i_g, i_l, and i_h are the grid current, load current, and shunt compensation current, respectively. Taking Kirchhoff's laws into account, the following relationships can be defined

$$e_g = v_{sh} + Z_g i_g, \tag{5.1}$$

Figure 5.1 – Proposed 4L-UPQC configuration.

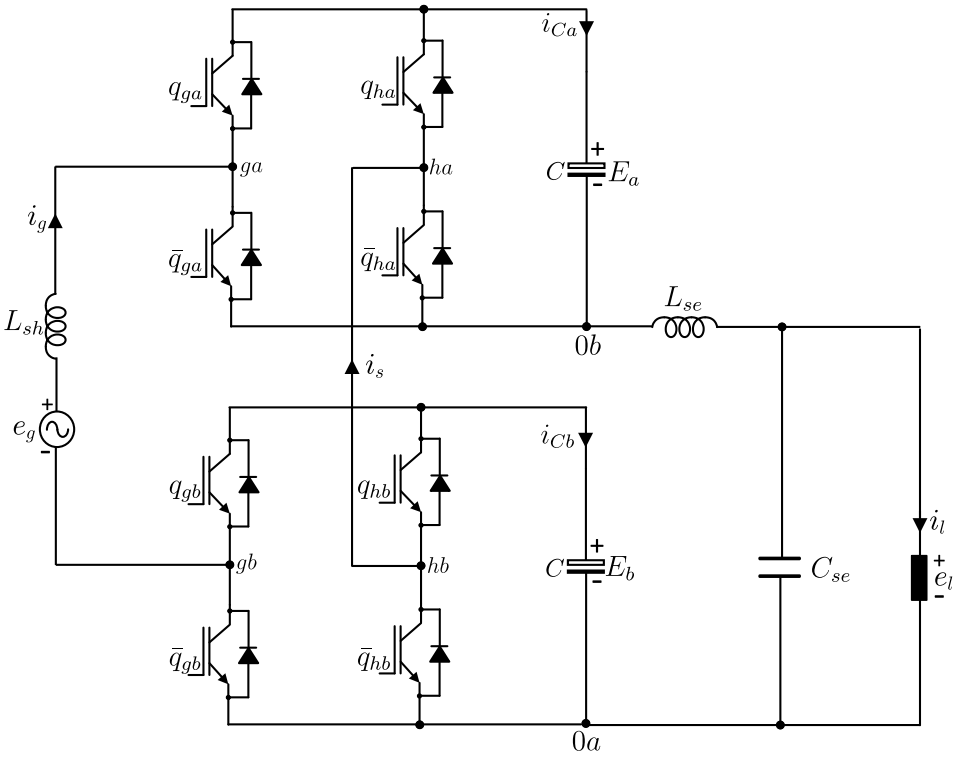
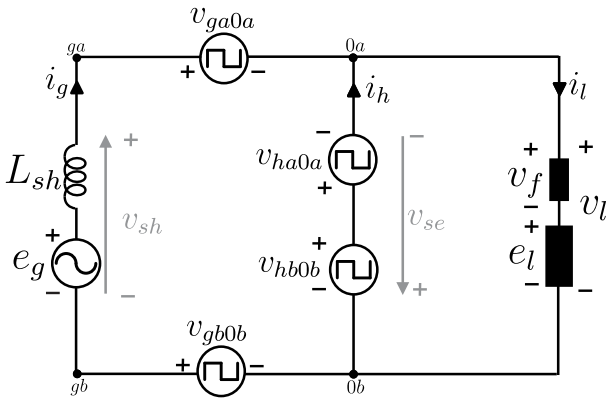


Figure 5.2 – Equivalent circuit.



$$e_l = -v_{se} + Z_f i_l, \tag{5.2}$$

$$i_h = i_l - i_g, \tag{5.3}$$

where $Z_{sh} = r_{sh} + \frac{d}{dt} l_{sh}$ and $Z_{se} = r_{se} + \frac{d}{dt} l_{se}$ represent the impedances of inductors L_{sh} and L_{se}, respectively. For the proposed topology, v_{sh} and v_{se} can be write as follows

$$v_{sh} = v_{ga0a} - v_{gb0b} + v_{hb0b} - v_{ha0a}, \tag{5.4}$$

$$v_{se} = v_{ha0a} - v_{hb0b}, \tag{5.5}$$

where v_{kj0j} is the pole voltage of the proposed configuration, which can be defined as $v_{kj0j} = q_{kj}E_j$. The switch q_{kj} represents the binary state of the upper switch of the leg k $(= g, h)$ and E_j is the dc-link voltage of dc-link j $(= a, b)$.

5.2 PWM Strategy

To control the proposed four-leg converter, this section presents a simplified scalar PWM. Since the desired reference voltages are represented as v^*_{sh} and v^*_{se}, the reference pole voltages are given by

$$v^*_{ha0a} - v^*_{hb0b} = v^*_{se} \tag{5.6}$$

$$v^*_{ga0a} - v^*_{gb0b} = v^*_{sh} + v^*_{se} \tag{5.7}$$

As can be seen, these equations can be solved if at least one reference pole voltage of each equation is specified.

5.2.1 Determination of v_{ha0a} and v_{hb0b}

As can be seen, (5.6) can be solved if v^*_{hb0b} is specified. Thus, one can rewrite as follows

$$v^*_{ha0a} = v^*_{se} + v^*_{\mu_h}, \tag{5.8}$$

$$v^*_{hb0b} = v^*_{\mu_h}, \tag{5.9}$$

where $v^*_{\mu_h}$ is a auxiliary variable. The maximum and minimum values for $v^*_{\mu_h}$ are defined using (5.8) and (5.9), considering the maximum ($E^* = E^*_a = E^*_b$) and minimum (0) values of each pole voltages [see Fig. 2(b)]. Therefore, the boundaries of $v^*_{\mu_h}$ are calculated by

$$v^*_{\mu_{h\,max}} = E^* - \max\{v^*_{se}, 0\}, \tag{5.10}$$

$$v^*_{\mu_{h\,min}} = -\min\{v^*_{se}, 0\}, \tag{5.11}$$

in which $E^* = E^*_a = E^*_b$ is the reference dc-link voltage of both h-bridges. The auxiliary variable can be normalized introducing the general apportioning factor μ_h $(0 \leq \mu_h \leq 1)$, such that

$$v^*_{\mu_h} = \mu_h v^*_{\mu_{h\,max}} + (1-\mu_h) v^*_{\mu_{h\,min}}. \tag{5.12}$$

After select μ_h, the auxiliary variable $v^*_{\mu_h}$ can be defined and the pole voltages v^*_{ha0a} and v^*_{hb0b} can be determined using (5.8) and (5.9).

5.2.2 Determination of v_{ga0a} and v_{gb0b}

It can be noticed that (5.7) can be solved if v^*_{gb0b} is specified. In the same way, one can rewrite as follows

$$v^*_{ga0a} = v^*_{sh} + v^*_{se} + v^*_{\mu_g}, \tag{5.13}$$

$$v^*_{gb0b} = v^*_{\mu_g}, \tag{5.14}$$

where $v^*_{\mu_g}$ is also a auxiliary variable. Their maximum and minimum values can be defined using (13) and (14). Thus, the boundaries of $v^*_{\mu_g}$ are calculated by

$$v^*_{\mu_{g\,max}} = E^* - \max\{v^*_{sh} + v^*_{se}, 0\}, \tag{5.15}$$

$$v^*_{\mu_{h\,min}} = -\min\{v^*_{sh} + v^*_{se}, 0\}, \tag{5.16}$$

The auxiliary variable $v^*_{\mu_g}$ can be normalized introducing the general apportioning factor μ_g ($0 \leq \mu_h \leq 1$), such that

$$v^*_{\mu_g} = \mu_g v^*_{\mu_{g\,max}} + (1-\mu_g) v^*_{\mu_{g\,min}}. \tag{5.17}$$

After select μ_g, the auxiliary variable $v^*_{\mu_g}$ can be defined and the pole voltages v^*_{ga0a} and v^*_{gb0b} can be determined using (5.13) and (5.14).

Once calculated the pole voltages, the gate command of the switches are defined applying a carrier-based PWM.

5.3 Operation Constraints

In the proposed 4L-UPQC configuration, the reference voltages v^*_{sh} and v^*_l can only be correctly synthesized if the dc-link voltages of the proposed 4L-UPQC obey the following condition

$$E = \sqrt{V_{sh}^2 + V_l^2 - 2V_{sh}V_l\cos(\epsilon)}, \tag{5.18}$$

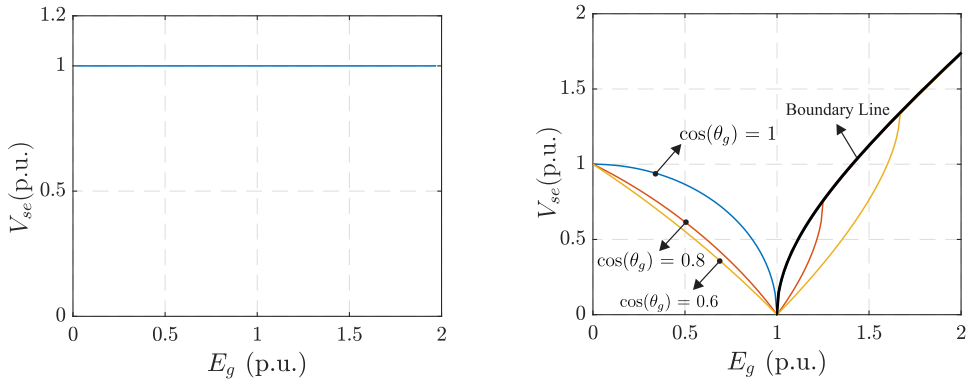
where ϵ is the phase angle between v_{sh}^* and v_l^* and $E = E_a = E_b$. According to (5.18), for a constant load voltage $V_l = 1$ pu and $E = 1$ pu, the proposed system is able to withstand voltage sags and swells until 100%, while it ensures shunt compensation. Fig. 5.3(a) presents the behavior of the series converter. As the series converter side is connected in parallel to the load, it remains constant equal to 1 pu and does not depends on the load power factor. Operating without a fixed source at the dc-link, i.e, using the minimum energy injection control, the conventional single-phase 4L-OPEN-UPQC presents operation constraints related of shunt compensation under voltage swells, as depicted in Fig. 5.3(b). One can notice that, under voltage swell transients, the 4L-OPEN-UPQC needs to decrease the grid power factor and increase its dc-link voltage, dealing with nonactive currents and increasing the switching power losses. Generalizing for any grid power factor value, the following equation can be defined for the dc-link voltage of the series module

$$E = \sqrt{V_l^2 - [E_g \cos(\theta_g)]^2} - E_g \sin(\theta_g), \tag{5.19}$$

where θ_g is the angle of the grid voltage. For correct operation, the following condition must be considered:

$$V_l \geq E_g \cos(\theta_g). \tag{5.20}$$

Figure 5.3 – Series converter voltage required. (a) Proposed 4L-UPQC, (b) Conventional 4L-OPEN-UPQC.

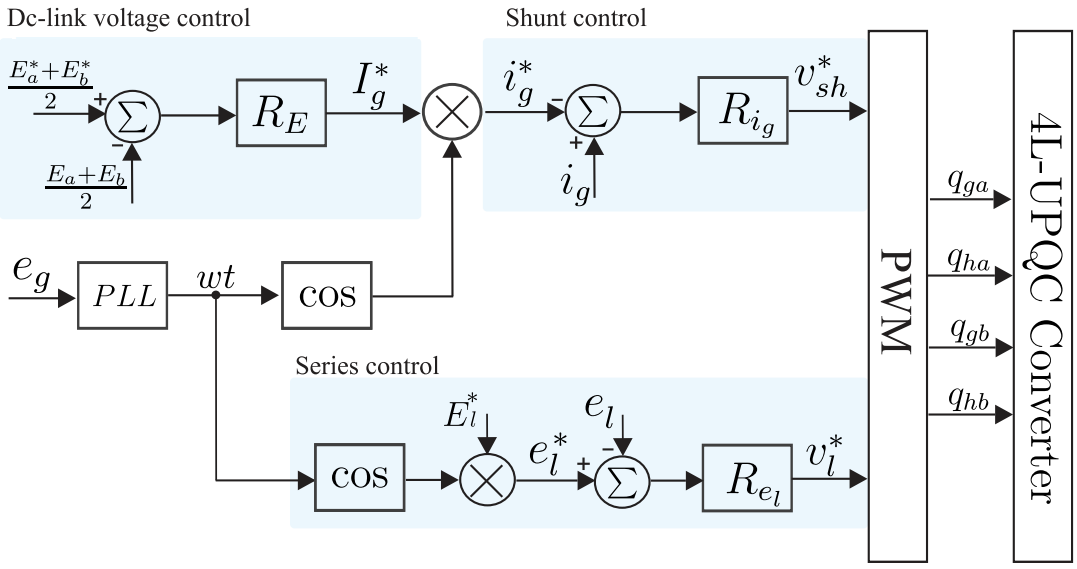


5.4 Control System

The control diagram for the proposed system is shown in Fig. 5.4. A proportional-integral (PI) controller labeled R_E is used to control the average dc-link voltage [$E_m = (E_a + E_b)/2$] and provides the amplitude of the grid current (I_g^*). The control considering the average value in the proposed structure is sufficient to ensure the correct dc-link voltages regulation for both h-bridge modules. For the load current $i_l \geq 0$, the connection

to the load allows the upper converter to discharge and the lower converter to charge. For $i_l < 0$, the upper converter charges and the lower one discharges. As the *ga* and *ha* legs behave identically to the *gb* and *hb* legs, it is to be expected that equalization will occur naturally. The blocks PLL (phase locked loop) and cos [cos(wt)] are responsible for generating the instantaneous grid current synchronized with the grid voltage (e_g) to ensure a grid power factor close to the unity. R_{ig} is a proportional resonant (PR) controller that receives the error i_g-i_g^* and generates the reference voltage of v_{sh}^*. In the same way, the block cos generates the reference load voltage e_l^* synchronized with e_g. R_{el} block, also a PR controller, is used to generate v_l^*.

Figure 5.4 – Block diagram of control strategy.



5.5 Results

The effectiveness of the proposed 4L-UPQC is demonstrated through both simulation and experimental results. The test setup includes SEMIKRON semiconductor power devices, specifically IGBTs and SKH23 gate drivers, along with a TMS320F28335 DSP from Texas Instruments. Unless made clear otherwise, the parameters used for these tests are listed in Table 5.1

5.5.1 Simulation Results

Simulation tests were performed to validate the performance of the proposed configuration as UPQC. First, the functionality of the proposed converter under simultaneous grid voltage and load current disturbances was verified. The grid voltage disturbances included third (10%), fifth (5%), and seventh (2%) order harmonics. A nonlinear load with

Table 5.1 – Parameters used in simulations and experimental tests.

Parameter		Value
Grid voltage	e_g	110 V rms 77 V rms 143 V rms
Load reference voltage	e_l^*	110 V rms
Switching frequency	f_s	10 kHz
Dc-link capacitor	C	2.2 mF
Dc-link voltage	E, E_h	180/180 V
Shunt inductance	L_{sh}	5 mH
Series filter inductance	L_{se}	1 mH
Series filter capacitance	C_{se}	120 μH
Series filter dump resistance	R_{se}	10 Ω
Nonlinear load		
Apparent Power 1	S_{l1}	0.62 kVA
Apparent Power 2	S_{l2}	0.92 kVA
Load current THD 2	THD_{il}	68 %
Load current THD 1	THD_{il}	51 %

approximately 68% harmonic distortion and 0.62 kVA was used in these tests. Figures 5.5, 5.6, and 5.7 show the following operating conditions, respectively: grid voltage under nominal conditions, 30% voltage sag, and 30% voltage swell, respectively. In all three scenarios, the converter effectively maintained grid power factor regulation, load voltage compensation, and dc-link voltage regulation. In addition, the grid current achieved a THD of less than 5%.

Next, simulation results are shown in Figures 5.8, 5.9, and 5.10, demonstrating the proposed converter's capability to compensate for harmonic and reactive currents, and to mitigate voltage sags and swells in the grid. Fig. 5.8 and 5.9 present the behavior of the proposed configuration under 30% of voltage swell and sag, respectively. In both cases, a typical single-phase full-bridge rectifier with THD(%) = 68% has been employed as nonlinear load (0.62 kVA/0.92 kVA). Throughout this process, the load voltage remains compensated. Notice that the proposed system is able to ensure shunt and series compensation under rated and transient conditions. Additionally, the effectiveness of the dc-link voltage control and the grid current control can be observed. Lastly, the effectiveness of the grid current and dc-link voltage controls was validated with a load power increase of approximately 47%. The results demonstrate that the dc-link voltages remain regulated at their steady-state values, indicating stable operation. Additionally, the grid voltage and current are in phase, ensuring a unity power factor.

Figure 5.5 – Simulation results of the proposed converter under nominal conditions. (a) Grid voltage with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic and grid current. (b) Load voltage and Load current. (c) Shunt compensation current. (d) Dc-link voltages E_a, E_b.

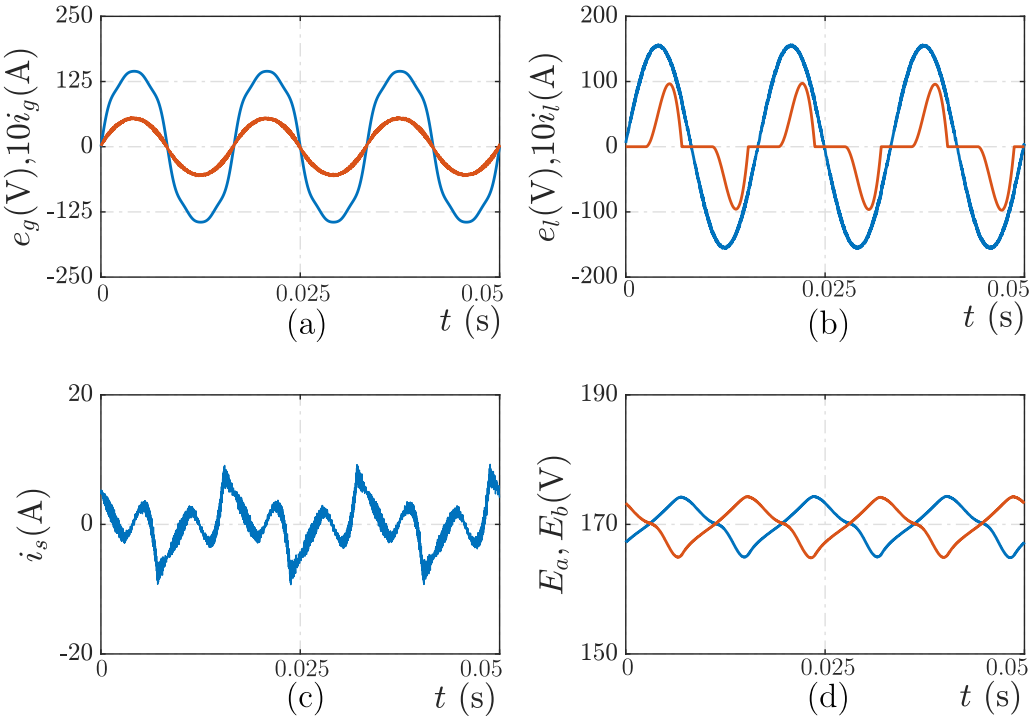


Figure 5.6 – Simulation results of the proposed converter under 30% of grid voltage sag. (a) Grid voltage with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic and grid current. (b) Load voltage and Load current. (c) Shunt compensation current. (d) Dc-link voltage E_a, E_b.

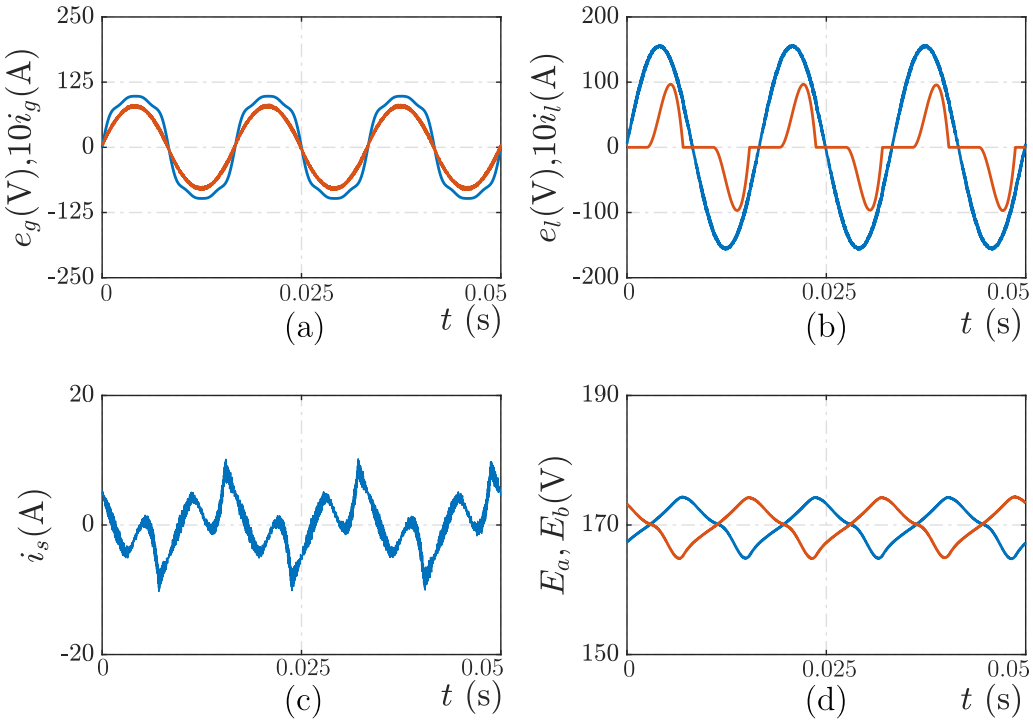


Figure 5.7 – Simulation results of the proposed converter under 30% of grid voltage swell. (a) Grid voltage with 10% of third harmonic, 5% of fifth harmonic, and 2% of seventh harmonic and grid current. (b) Load voltage and Load current. (c) Shunt compensation current. (d) Dc-link voltage E_a, E_b.

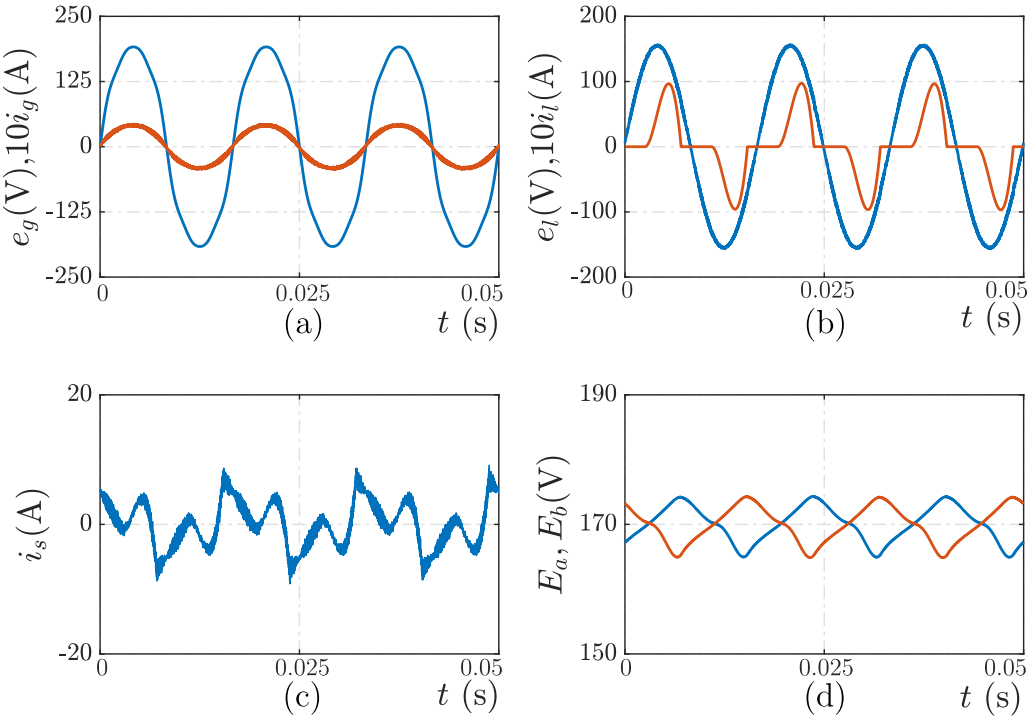
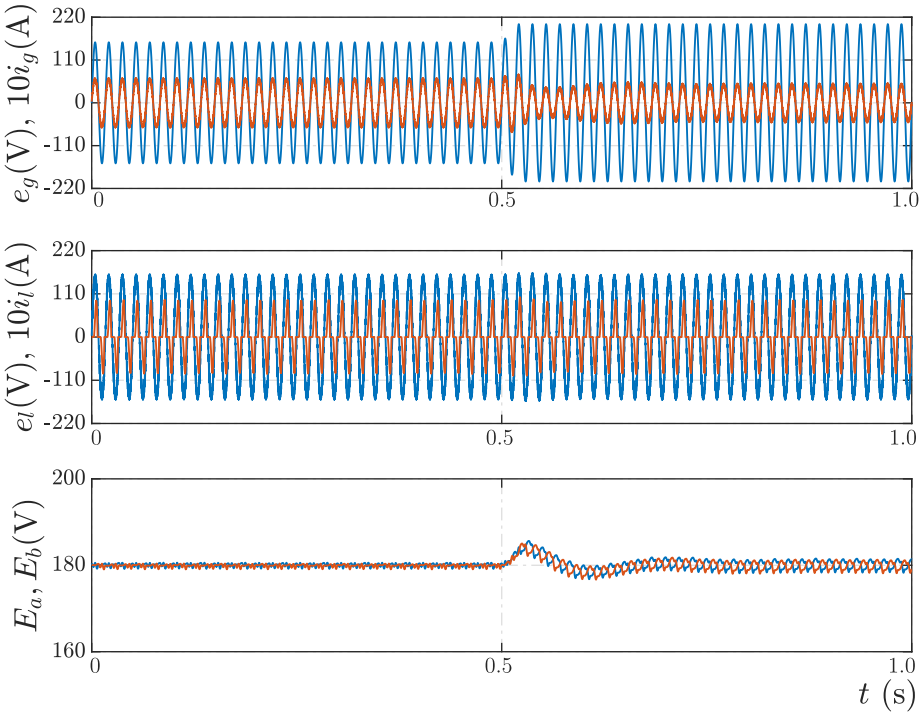


Figure 5.8 – Simulation results of the proposed converter under a voltage swell of 30%.



5.5.2 Experimental Results

To validate the simulation tests, experimental results were performed for the proposed 4L-UPQC configuration. Figs 5.11, 5.12, 5.13, and 5.14 present experimental

Figure 5.9 – Simulation results of the proposed converter under a voltage sag of 30%.

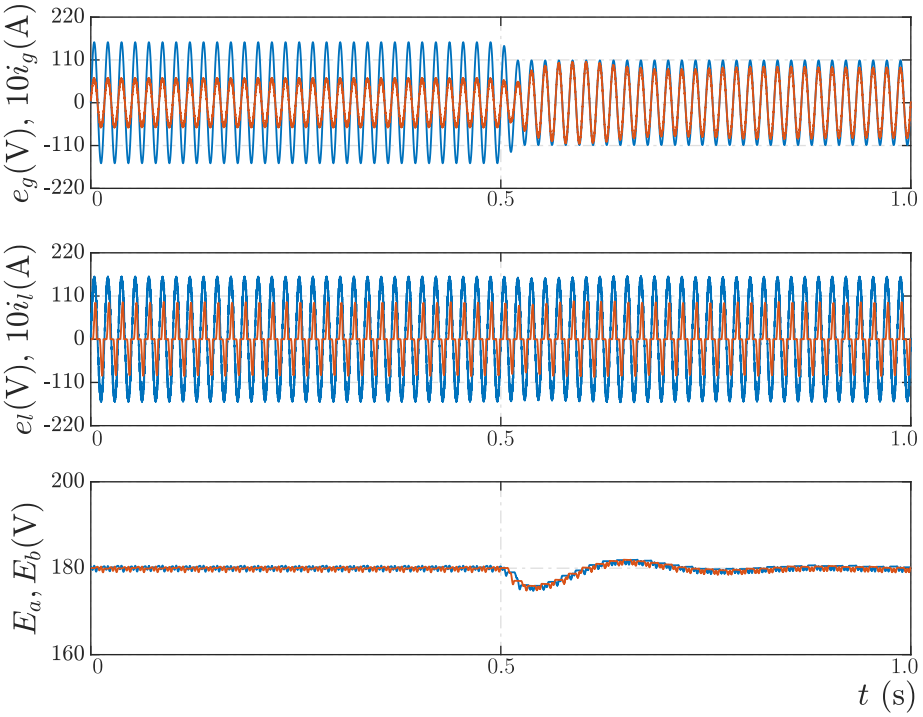
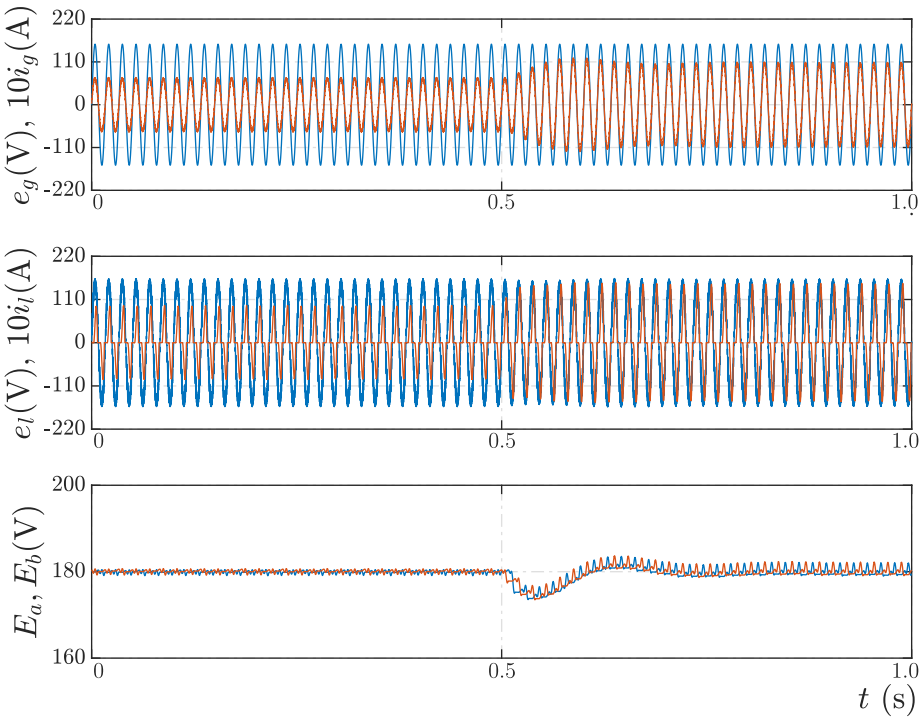


Figure 5.10 – Simulation results of the proposed converter under rated conditions with a step in the load power from $S_l = 0.62$ kVA to $S_l = 0.92$ kVA.



results for the proposed converter operating under grid voltage disturbances and load step. Fig. 5.11 and 5.12 demonstrate the capability of the proposed converter to compensate 30% of voltage swell and sag, respectively. It can be observed that the dc-link voltages and the load voltage kept controlled. Next, Fig. 5.13 and 5.14 depict a transient caused by an

active load power increase of 47%. As can be seen, converter ensured load voltage control before and during the transient. The increase in the load current generated an increase in the grid current to adjust the dc-link voltages.

Figure 5.11 – Experimental results - Grid voltage swell of 30%. Grid (e_g) and load (e_l) voltages and dc-link voltages (E_a and E_b) with zoomed view (a) before of the disturbance, (b) in the beginning of the disturbance, and (c) during the disturbance.

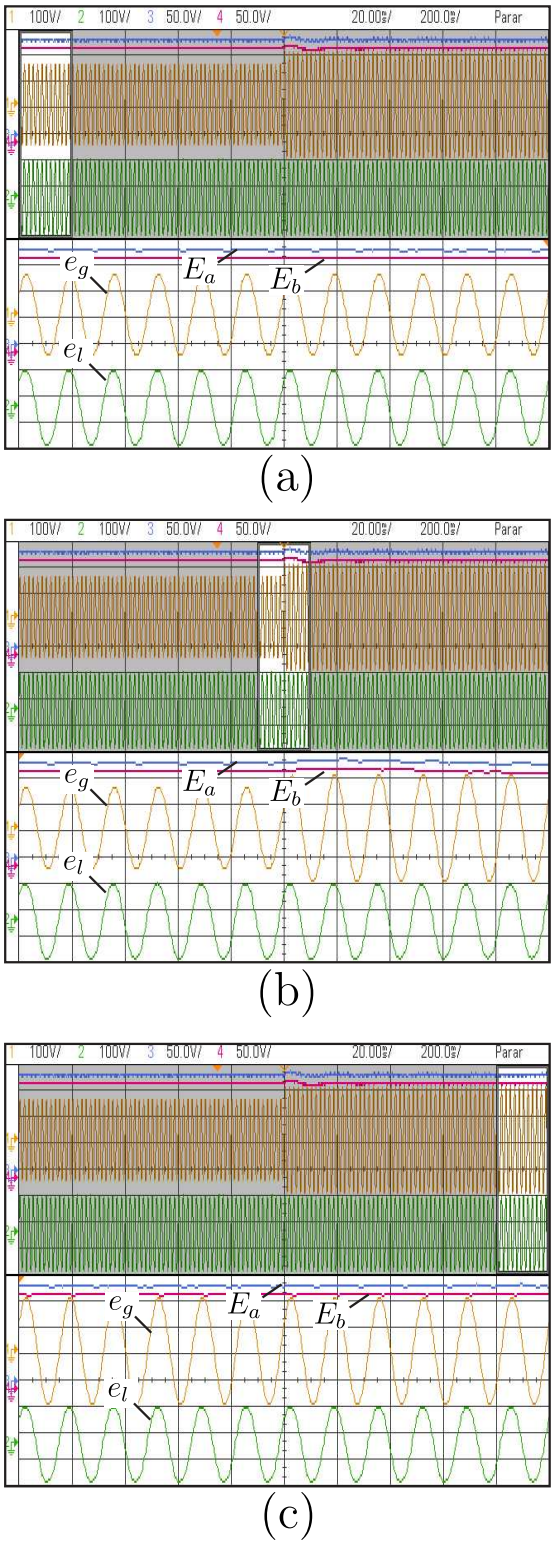
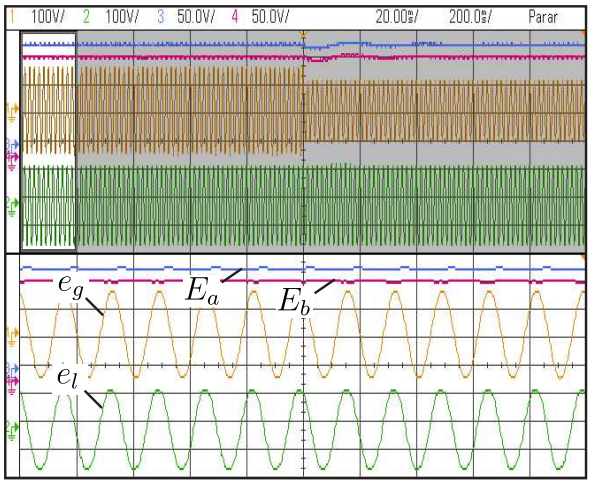
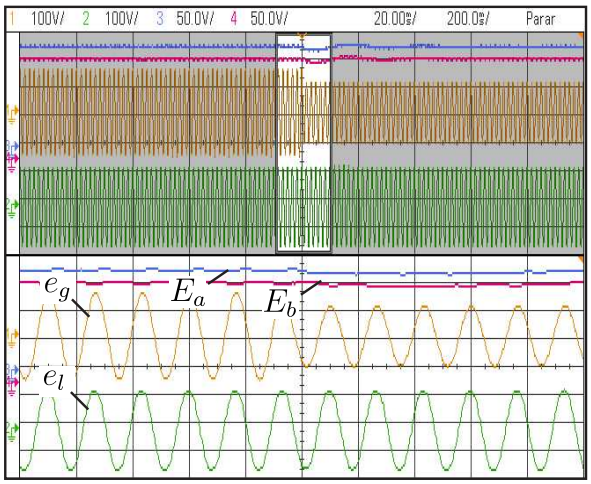


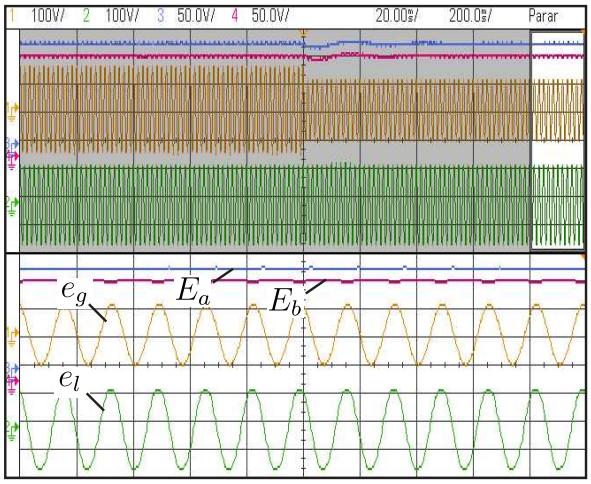
Figure 5.12 – Experimental results - Grid voltage sag of 30%. Grid (e_g) and load (e_l) voltages and dc-link voltages (E_a and E_b) with zoomed view (a) before of the disturbance, (b) in the beginning of the disturbance, and (c) during the disturbance.



(a)

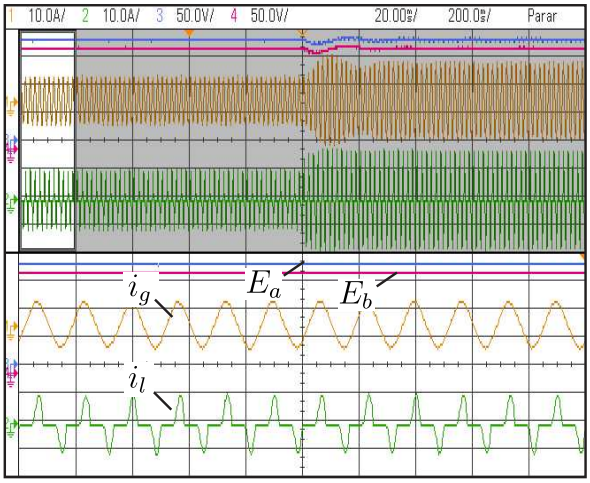


(b)

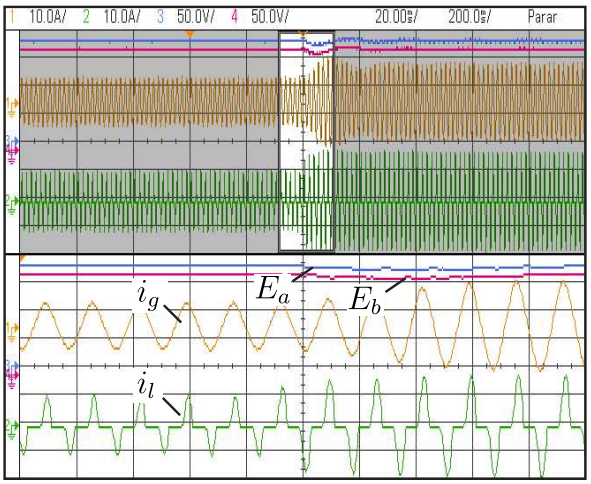


(c)

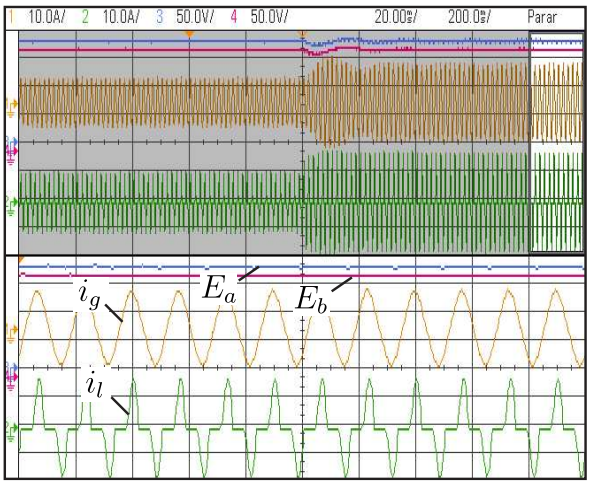
Figure 5.13 – Experimental results of the proposed converter under rated conditions with a step in the load power from $S_l = 0.62$ kVA to $S_l = 0.92$ kVA. Grid (i_g) and load (i_l) currents and dc-link voltages (E_a and E_b) with zoomed view (a) before of the disturbance, (b) in the beginning of the disturbance, and (c) during the disturbance.



(a)

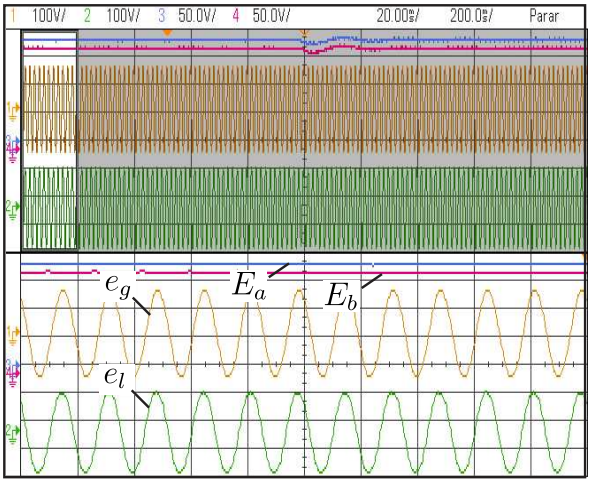


(b)

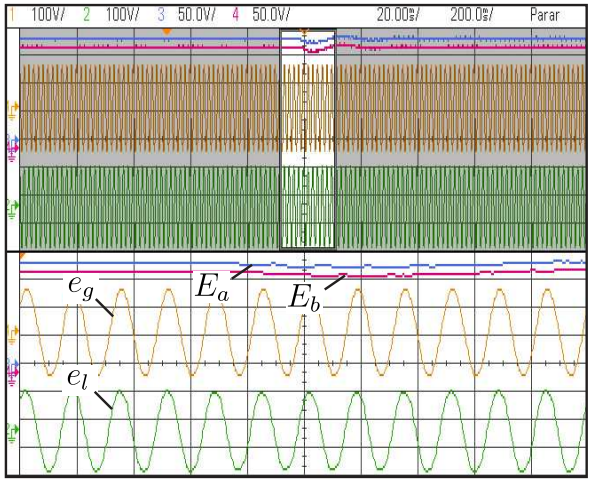


(c)

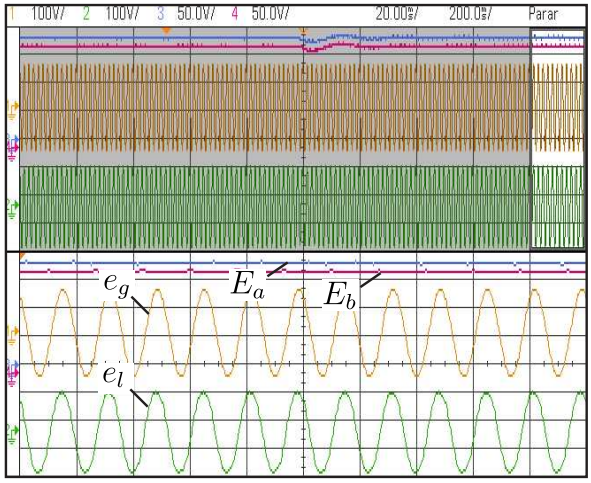
Figure 5.14 – Experimental results of the proposed converter under rated conditions with a step in the load power from $S_l = 0.62$ kVA to $S_l = 0.92$ kVA. Grid (e_g) and load (e_l) voltages and dc-link voltages (E_a and E_b) with zoomed view (a) before of the disturbance, (b) in the beginning of the disturbance, and (c) during the disturbance.



(a)



(b)



(c)

5.6 Comparison of the Topologies

This section compares the proposed 4L-UPQC configuration with the transformerless configurations studied in the previous chapter, named 3LS-UPQC, SB-3L-UPQC, and 3L-SH-UPQC. The configurations are evaluated based on the reverse voltage on the power switches, harmonic distortion, and power losses. Unless made clear otherwise, the tests were made with the parameters shown in Table 5.2. Three different cases are considered when analyzing the harmonic distortion and power losses:

- Case A - Rated condition;
- Case B - 50% grid voltage swell;
- Case C - 50% grid voltage sag.

Table 5.2 – Parameters considered for the tests.

Parameter		Value
Rated load power	P_l	1 kW
Load power factor	$\cos(\delta_l)$	0.7 lagging
Reference load voltage amplitude	E_l^*	155.6 V
Grid voltage amplitude	E_g	155.6 V
Dc-link voltage - 3L-SH-UPQC	E, E_h	170/75 V
Dc-link voltage - 4L-UPQC	E_a, E_b	180/180 V
Dc-link voltage - 3LS-UPQC	E	196 V
Dc-link voltage - SB-3LS-UPQC	E, E_s	196/170 V
Switching frequency	f_s	10 kHz
Grid and load frequency	f_g/f_l	60/60 Hz
Three-leg shunt inductance	L_s	5 mH
Hybrid shunt inductance	L_h	5 mH
Hybrid shunt capacitance	C_h	266 μF
Series filter inductance	L_f	2 mH
Series filter capacitance	C_f	18 μH
Series filter dump resistance	R_f	10 Ω
Dc-link capacitor	C	2.2 mF

5.6.1 Rating of the Semiconductor Devices

Table 5.3 shows the reverse voltage on the power switches for the four studied converters. For the proposed 4L-UPQC, the value of the dc-link voltage depends only on the range of the grid voltage sag and swell that the converter is designed to support, as there is no dependence on the load characteristics. Considering that the 4L-UPQC is designed to support up to 1 p.u., at least 1 p.u. is required in each h-bridge module when considering operation with unity modulation index in the grid side under nominal conditions. The

values given in Table 5.3 for 4L-UPQC were set at 0.87 to avoid compromising the load voltage waveform due to the dc-link voltage ripple.

Table 5.3 – Rating of the semiconductor devices.

3L-SH-UPQC					
Switch	q_g	q_l	q_s	q_{ha}	q_{hb}
Voltage (p.u.)	1.09	1.09	1.09	0.48	0.48
4L-UPQC					
Switch	q_{ga}	q_{sa}	q_{gb}	q_{sb}	
Voltage (p.u.)	1.15	1.15	1.15	1.15	
3LS-UPQC					
Switch	q_g	q_l	q_s		
Voltage (p.u.)	1.26	1.26	1.26		
SB-3LS-UPQC					
Switch	q_g	q_l	q_a	q_{s1}	q_{s2}
Voltage (p.u.)	1.26	1.26	1.26	1.09	1.09

*1 p.u. = 155.6 V

5.6.2 Harmonic Distortion

The total harmonic distortion (THD) of the grid currents (i_g) and load voltage (e_l) have been calculated to compare the 4L-PUC with the investigated configurations in the previous chapter. In this way, The THD can be defined as follows

$$THD(\%) = \frac{100}{\sigma_1}\sqrt{\sum_{n=2}^{N_x}\sigma_n^2} \tag{5.21}$$

where σ_1 is the amplitude of the fundamental component, σ_n is the amplitude of the harmonic of order n, and N_x is the number of harmonics that are used in the calculation. The THD and WTHD were obtained using $N_x = 1000$ components. Table 5.4 shows the THD for the four studied configurations. It can be seen that the four configurations achieved similar results in all analyzed scenarios. This is due to the fact that the dc-link voltage values of the analyzed configuration are not very different at this simulated operating point and the converters generate a similar number of levels on the series and shunt sides. The harmonic content for i_g and e_l in the 3LS-UPQC and SB-3LS-UPQC configurations became more evident at higher load powers and lower power factors scenarios (see Fig. 4.3).

5.6.3 Power Losses

The power losses of the configurations investigated in this section were calculated using the thermal modules of the PSIM V9.1 software. The IGBT SKM50GB063D from

Table 5.4 – THD analysis.

Case A		
Converter	THD (%)	
	i_g	e_l
3L-SH-UPQC	1.49	1.01
4L-UPQC	1.45	1.05
3LS-UPQC	1.71	1.07
SB-3LS-UPQC	1.84	1.12
Case B		
Converter	THD (%)	
	i_g	e_l
3L-SH-UPQC	4.18	3.16
4L-UPQC	3.98	3.18
3LS-UPQC	4.05	3.29
SB-3LS-UPQC	4.12	3.35
Case C		
Converter	THD (%)	
	i_g	e_l
3L-SH-UPQC	0.90	2.18
4L-UPQC	0.74	2.22
3LS-UPQC	0.95	2.35
SB-3LS-UPQC	1.01	2.39

Semikron was used as the power switch in the analysis. The power loss calculations considered the conduction losses (P_{cd}), switching losses (P_{sw}) and the total power losses ($P_t = P_{cd} + P_{sw}$). Operating points for three different power values (0.5 kW, 1 kW, and 2 kW) and two different voltage levels (110 V/220 V) were selected to verify the scenarios in which each topology stands out. The Tables 5.5, 5.6, 5.7, 5.9, 5.9, and 5.10 show the power losses for the following scenarios:

- 0.5 kW/ 110 V (Table 5.5)
- 1.0 kW/ 110 V (Table 5.6)
- 2.0 kW/ 110 V (Table 5.7)
- 0.5 kW/ 220 V (Table 5.8)
- 1.0 kW/ 220 V (Table 5.9)
- 2.0 kW/ 220 V (Table 5.10)

As can be seen, the proposed 4L-UPQC shows a better performance under rated conditions and especially under grid voltage swell scenarios, presenting similar overall power losses than 3LS-UPQC and 3LS-SH-UPQC. On the other hand, this structure and

SB-3LS-UPQC showed the worst results under all scenarios of grid voltage sags. This occurred because both structures, compared to 3LS-UPQC and 3LS-SH-UPQC, have more legs operating with the grid current. In this context, it is noted that the proposed 4L-UQPC has a tendency to stand out in power losses under high voltage and low current scenarios.

As already mentioned, it is important to highlight that, unlike the 4L-UPQC and 3LS-SH-UPQC, the design of the dc-link voltage value of 3LS-UPQC and SB-3LS-UPQC depends on the load power characteristics, which can lead to operation with a low modulation index, as shown in Fig. 4.3. Therefore, the 4L-UPQC and 3LS-SH-UPQC configurations are the most promising of the investigated configurations in terms of losses. However, in terms of the complexity of implementation, for proper operation, the 3LS-SH-UPQC configuration requires additional control loops and voltage and current sensors, which increase the complexity of the overall control system compared to the 4L-UPQC configuration.

Table 5.5 – Semiconductor power losses - 0.5 kW - 110V.

Case A			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	11.4	12.9	24.3
4L-UPQC	10.4	12.8	23.2
3LS-UPQC	12.1	12.4	24.5
SB-3LS-UPQC	15.8	12.4	28.2
Case B			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	10.8	17.2	28.0
4L-UPQC	8.4	11.9	20.3
3LS-UPQC	11.3	18.2	29.5
SB-3LS-UPQC	12.5	18.1	30.6
Case C			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	19.4	17.9	37.3
4L-UPQC	25.6	22.7	48.3
3LS-UPQC	18.4	17.5	35.9
SB-3LS-UPQC	33.8	18.48	52.28

Table 5.6 – Semiconductor power losses - 1 kW - 110V.

Case A			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	28.7	19.3	48.0
4L-UPQC	27.2	18.0	45.2
3LS-UPQC	24.6	24.1	48.6
SB-3LS-UPQC	36.9	24.3	61.2
Case B			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	26.4	25.2	51.6
4L-UPQC	22.0	20.0	42.0
3LS-UPQC	22.0	30.9	53.0
SB-3LS-UPQC	28.9	31.3	60.2
Case C			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	49.3	32.5	81.9
4L-UPQC	69.9	51.0	120.9
3LS-UPQC	42.2	37.7	79.9
SB-3LS-UPQC	61.6	38.0	99.6

Table 5.7 – Semiconductor power losses - 2 kW - 110V.

Case A			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	71.1	49.6	120.7
4L-UPQC	68.9	51.5	120.4
3LS-UPQC	61.8	64.8	126.6
SB-3LS-UPQC	101.2	54.0	155.2
Case B			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	58.8	49.5	108.3
4L-UPQC	55.2	42.5	97.7
3LS-UPQC	55.4	74.7	130.1
SB-3LS-UPQC	77.2	68.0	145.2
Case C			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	133.7	93.2	226.9
4L-UPQC	238.7	138.9	377.6
3LS-UPQC	112.1	100.0	212.1
SB-3LS-UPQC	225.6	102.3	327.9

Table 5.8 – Semiconductor power losses - 0.5 kW - 220V.

Case A			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	4.6	22.3	26.9
4L-UPQC	3.2	19.7	22.2
3LS-UPQC	5.0	17.9	22.9
SB-3LS-UPQC	6.1	19.0	25.1
Case B			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	4.8	31.7	36.5
4L-UPQC	2.5	19.7	22.2
3LS-UPQC	5.3	28.8	34.1
SB-3LS-UPQC	6.5	31.5	38.0
Case C			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	8.0	27.3	35.3
4L-UPQC	9.1	24.9	34.0
3LS-UPQC	7.5	21.4	28.9
SB-3LS-UPQC	12.6	21.9	34.5

Table 5.9 – Semiconductor power losses - 1 kW - 220V.

Case A			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	11.3	27.5	38.8
4L-UPQC	9.3	25.1	34.4
3LS-UPQC	12.0	24.7	36.7
SB-3LS-UPQC	15.2	24.8	40.0
Case B			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	11.1	38.2	49.3
4L-UPQC	7.4	23.9	31.3
3LS-UPQC	11.6	37.4	49.0
SB-3LS-UPQC	13.1	37.9	51.0
Case C			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	19.1	38.0	57.1
4L-UPQC	23.3	42.5	65.8
3LS-UPQC	9.5	21.4	30.9
SB-3LS-UPQC	31.5	35.0	66.5

Table 5.10 – Semiconductor power losses - 2 kW - 220V.

Case A			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	27.7	45.9	73.6
4L-UPQC	25.3	45.3	70.6
3LS-UPQC	26.6	47.8	74.4
SB-3LS-UPQC	38.3	47.4	85.7
Case B			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	26.2	55.1	81.3
4L-UPQC	20.5	38.1	58.6
3LS-UPQC	25.8	66.2	92.0
SB-3LS-UPQC	30.5	64.5	95.0
Case C			
Converter	P_{cd} (W)	P_{sw} (W)	P_t (W)
3L-SH-UPQC	46.7	70.2	116.9
4L-UPQC	59.9	90.9	150.8
3LS-UPQC	43.9	70.1	114.0
SB-3LS-UPQC	78.4	73.3	151.7

5.7 Conclusion

In this chapter, a single-phase transformerless converter for application as a UPQC was proposed. The configuration is based on two h-bridge modules. The load connection method allows natural dc-link balancing, simplifying the design of the control strategy compared to conventional transformerless UPQC systems. It was verified that, the proposed 4L-UPQC demonstrated a better performance under rated conditions and especially under grid voltage swell scenarios, presenting similar overall power losses than 3LS-UPQC and 3LS-SH-UPQC. On the other hand, this structure showed the worst results under all scenarios of grid voltage sags. This occurred because both structures, compared to 3LS-UPQC and 3LS-SH-UPQC, has more legs operating with the grid current. In this context, it was concluded that the proposed 4L-UQPC has a tendency to stand out in power losses under high voltage and low current scenarios. Although the decoupled method improves the overall performance of the three-leg converter (3LS-UPQC, 3LS-SH-UPQC, and SB-3LS-UPQC), this approach increases the complexity of the control system. In this context, the proposed 4L-UPQC is the most promising configuration presented in this work, as it does not have additional control loops or any other topological reconfiguration under transients. The experimental tests demonstrated that the proposed system ensures grid power factor compensation, dc-link voltage regulation, and sag and swell mitigation.

Chapter 6

Three-Phase Four-Wire Transformerless Unified Power Quality Conditioner Based on AC-DC-AC Nine-Leg Converter and Shunt Converter

6.1 Introduction

In the last years, the increasing use of semiconductor-based electronic equipment connected to the power grid has brought new challenges to creating power electronics solutions to mitigate issues, such as sags, swells, flickers, reactive power, harmonics, and unbalanced disturbances (YADAV; PATEL; MATHUR, 2020; RAY; RAY; DASH, 2022). In this context, several three-phase converters operating as unified power quality conditioners (UPQC) have been proposed in the technical literature (KHADKIKAR, 2012; BRENNA; FARANDA; TIRONI, 2009; DEVASSY; SINGH, 2018). When compared with equipment such as series or shunt active power filters (APF) (SHARMA; VERMA, 2021; ROY; BHATTACHARYA; CHATTERJEE, 2024; JúNIOR; JACOBINA; FABRICIO, 2023) and dynamic voltage restorer (DVR) (HASAN et al., 2021; KHERGADE et al., 2020), the UPQC systems stand out since they can deal with voltage and current disturbances simultaneously (LU et al., 2016; KWON; KWON; KWON, 2018).

Conventional UPQC systems are composed of two three-phase voltage source inverters (VSIs), a common dc link, LC filters, and line-frequency transformers (LFT) (KHADKIKAR, 2012). To improve cost and volume, transformerless and high-frequency

transformer-based UPQC topologies were presented (CHANG; CHANG; CHIANG, 2006; FELINTO; CUNHA; JACOBINA, 2022; ABDALAAL; HO, 2022; CHEUNG et al., 2017). In (VENKATRAMAN; SELVAN, 2017; PENG et al., 2016), transformerless UPQC systems composed of shunt and series compensators without a common dc link were proposed. These converters can decouple the shunt and series controls, however, when the system operates under voltage sag, auxiliary dc sources are required to supply the dc links. Besides that, load phase jump under voltage transients are present and operation with unity grid power factor under voltage sags compensation is not allowed.

In (CHANG; CHANG; CHIANG, 2006), a transformerless UPQC based on three single-phase ac-dc-ac three-leg modules is proposed. It can compensate voltage sags without an auxiliary dc source, and without generating voltage phase jumps on the load voltages, which commonly appear when conventional DVRs perform voltage compensations without dc sources (MEYER et al., 2008). However, issues related to the dc-link voltage regulation in scenarios with unbalanced loads or unbalanced voltage disturbances were found. For scenarios with unbalanced power distribution among phases, the dc-link voltage of this topology needs to be increased to allow its dc-link voltage balance. To solve this limitation, solutions connecting the three dc links were proposed (MAIA et al., 2018; CARDOSO et al., 2024). In, (MAIA et al., 2018), a converter with a single dc link was derived from the topology in (CHANG; CHANG; CHIANG, 2006). However, it requires open-ended connections both at grid and load. Open-ended connections are not commonly found in the power systems, which may limit the application of this solution, or may require additional low frequency transformers to make it feasible. In (CARDOSO et al., 2024) it has been proposed a solution connecting the three dc links using a dc-dc converter with a HFT.

In this chapter, a three-phase transformerless UPQC based on a nine-leg converter and a four-wire shunt converter is proposed. The system ensures grid power factor compensation with low harmonic content and feeds the load with a sinusoidal waveform. The shunt converter provides balanced currents, which allows the nine-leg converter to operate with a wide range of unbalanced loads, while compensating for the harmonic content. In addition, the shared-leg currents are minimized, reducing the power losses. Compared with the conventional transformerless UPQCs, the proposed converter achieved lower overall semiconductor losses under a severely unbalanced load. The system model, pulse-width modulation (PWM) techniques, and control strategy are discussed in this work. Simulations and experimental results are presented to confirm the feasibility of the proposed structure and the correctness of the design methodology.

6.2 System Model

Fig. 6.1 shows the proposed three-phase UPQC (9LS-UPQC). The configuration is constituted by a three-leg module per phase, a four-leg shunt module, inductor and capacitor filters (L_g, L_l, L_h, and C_l), and four dc-link capacitors. The switches which form the structure are q_{gj}-$\bar{q}_{gj}$, q_{lj}-$\bar{q}_{lj}$, q_{sj}-$\bar{q}_{sj}$, q_{hj}-$\bar{q}_{hj}$, and q_{h4}-$\bar{q}_{h4}$, with $j = \{1,2,3\}$. The switching state is defined by 0 or 1, where $q_{gj} = 1$ denotes a closed switch and $q_{gj} = 0$ indicates an open switch. Fig. 6.2 presents the equivalent circuit of the proposed converter. Applying Kirchhoff's laws, the per-phase voltages and currents of the nine-leg converter can be obtained as follows

$$e_{gj} = Z_g i_{gj} + v_{gj}, \tag{6.1}$$

$$e_{lj} = v_{lj} - Z_l i_{lj}, \tag{6.2}$$

$$i_{gj} = i_{sj} + i_{fj}, \tag{6.3}$$

where i_{gj}, i_{fj}, i_{sj}, are the per-phase grid currents, nine-leg output currents, and shared-leg currents, respectively. $Z_g = R_g + \gamma L_g$ and $Z_l = R_l + \gamma L_l$ are the impedances of inductors L_g and L_l, respectively, with $\gamma = d/dt$. e_{gj}, e_{lj}, v_{gj}, and v_{lj} are the grid voltages, load voltages, converter voltages at grid side, and converter voltages at load side, respectively. The voltages v_{gj} and v_{lj} can be derived as

$$v_{gj} = v_{rj} - v_{gs}, \tag{6.4}$$

$$v_{lj} = v_{lj0j} - v_{sj0j}, \tag{6.5}$$

where v_{rj} are the per-phase converter resultant pole voltages at the grid side that is defined as $v_{rj} = v_{gj0_j} - v_{sj0_j}$; v_{gs} is the common-mode voltage which is determined by $v_{gs} = (v_{r1}+v_{r2}+v_{r3})/3$ considering a balanced three-phase three-wire grid (i.e., $e_{g1}+e_{g2}+e_{g3} = 0$). Additionally, v_{gj0_j}, v_{sj0_j}, and v_{lj0_j} are the pole voltages of the nine-leg converter, which are obtained by $v_{gj0_j} = (2q_{gj} - 1)E_j/2$, $v_{lj0_j} = (2q_{lj} - 1)E_j/2$, and $v_{sj0_j} = (2q_{sj} - 1)E_j/2$. E_j are the dc-link voltages of the nine-leg converter.

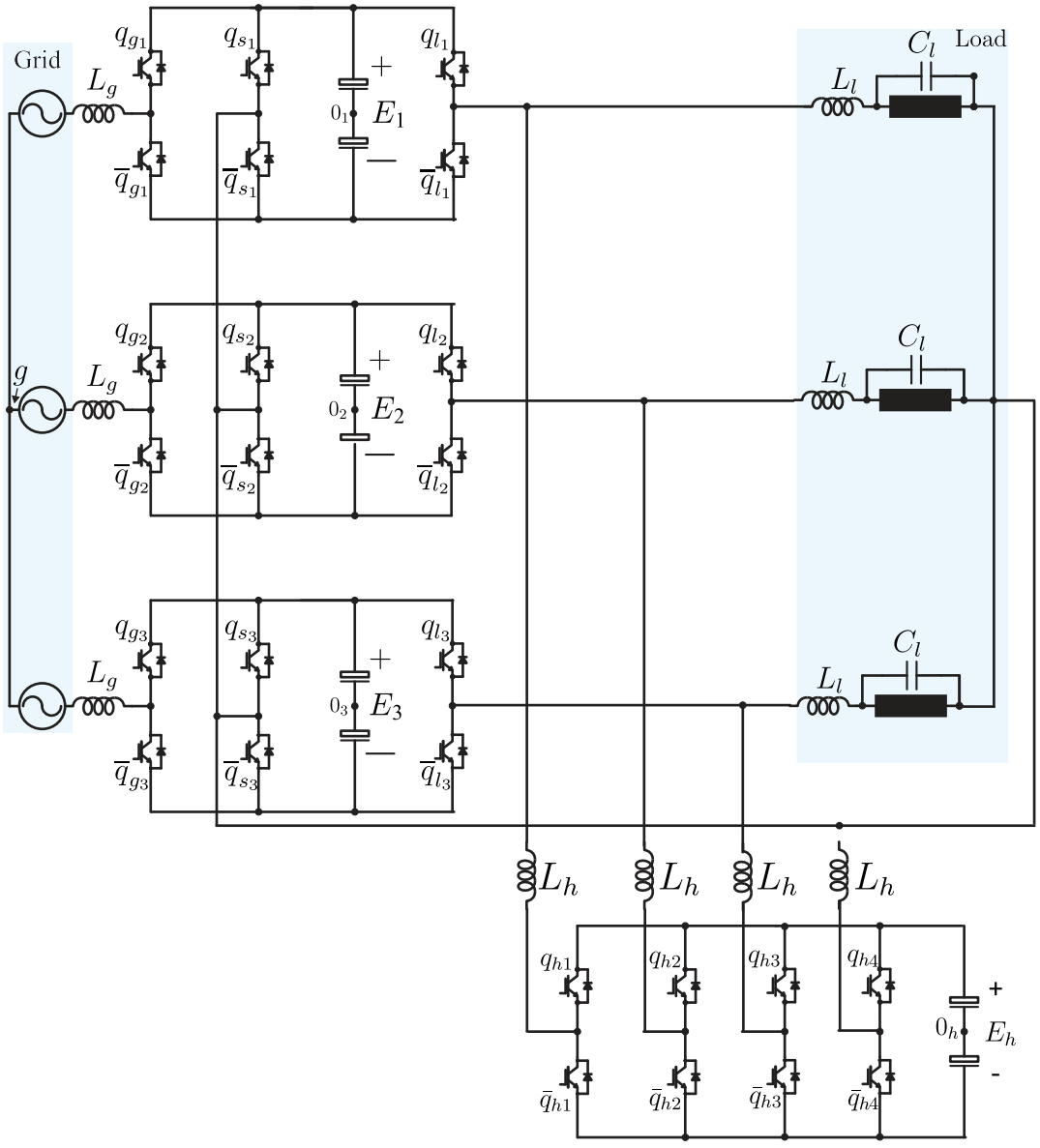
Considering the shunt converter, the per-phase voltages and currents according Kirchhoff's law are

$$v_{lj} = -Z_h i_{hj} + v_{hj}, \tag{6.6}$$

$$i_{hj} = i_{lj} - i_{fj}, \tag{6.7}$$

where i_{hj} are shunt compensation currents and $Z_h = R_h + \gamma L_h$. v_{hj} are the per-phase voltages across the shunt converter and they are defined as $v_{hj} = v_{hj0_h}$ - v_{l0_h}, with $v_{hj0_h} = (2q_{hj} - 1)E_h/2$ and $v_{l0_h} = (v_{h10_h} + v_{h20_h} + v_{h30_h} + v_{h40_h})/4$. The pole voltage of the fourth leg is defined as $v_{h40_h} = (2q_{h4} - 1)E_h/2$. E_h is the dc-link voltage of the shunt converter.

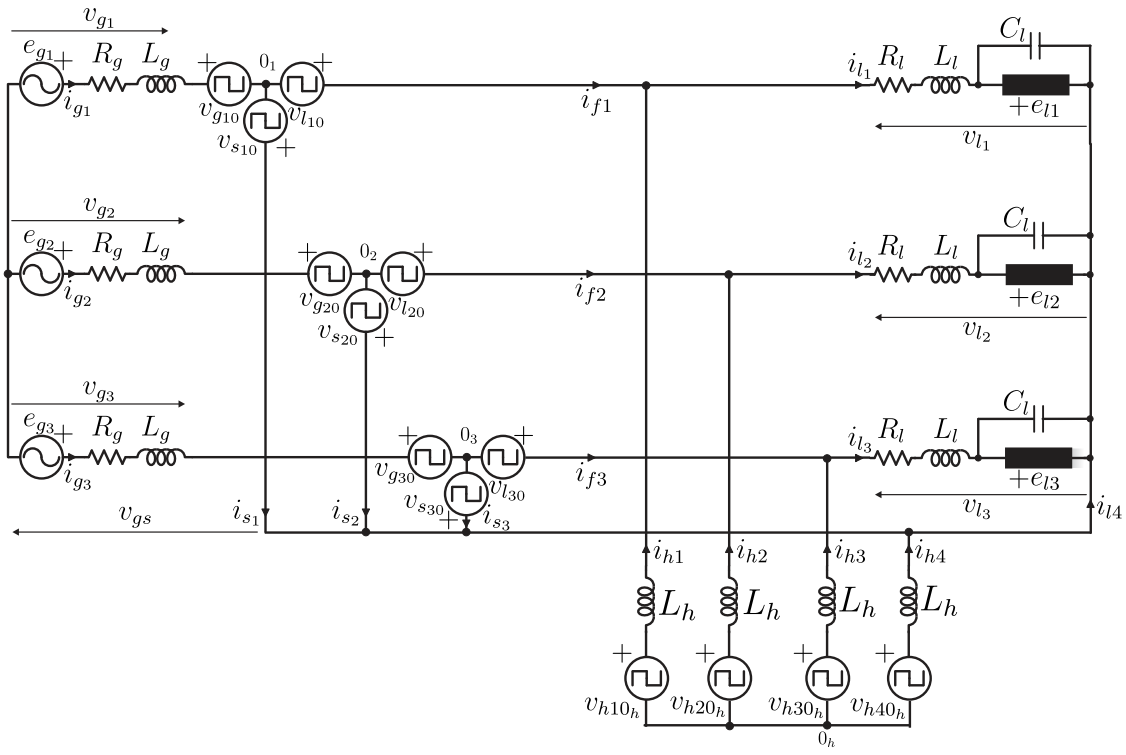
Figure 6.1 – Proposed 9LS-UPQC configuration.



6.3 PWM Strategy

To control the nine-leg and shunt converters, the PWM strategies are implemented in an independent way.

Figure 6.2 – Equivalent circuit.



6.3.1 Nine-leg Converter

Henceforward, the reference variables are indicated by the symbol * in the superscript. To control the nine-leg converter, a Space Vector PWM technique is developed. The desired per-phase reference voltages in the grid side (v^*_{rj}) is defined as

$$v^*_{rj} = v^*_{gj} + v^*_{gs}. \tag{6.8}$$

The input reference voltages v^*_{gj} are defined by the current controllers and the common-mode reference voltage v^*_{gs} is obtained using the third-harmonic injection technique. In this way, the local maximums and minimums are given by

$$v_{gs_{max}j} = \begin{cases} E^* - v^*_{gj}, & \text{if } v^*_{lj} \geq 0 \\ E^* - v^*_{gj} + v^*_{lj}, & \text{otherwise} \end{cases} \tag{6.9}$$

$$v_{gs_{min}j} = \begin{cases} -E^* - v^*_{gj}, & \text{if } v^*_{lj} \geq 0 \\ -E^* - v^*_{gj} + v^*_{lj}, & \text{otherwise} \end{cases} \tag{6.10}$$

Introducing the general apportioning factor μ^* ($0 \leq \mu^* \leq 1$), the reference common-mode voltage v^*_{gs} can be calculated as

$$v_{gs}^{*} = \mu^{*} V_{max} + (1 - \mu^{*}) V_{min}, \tag{6.11}$$

where $V_{max} = \min\{v_{gs_{max}j}\}$ and $V_{min} = \max\{v_{gs_{min}j}\}$.

Once defined, v_{rj}^{*} and v_{lj}^{*}, these voltages can be mapped in vector planes v_{rj}^{*} x v_{lj}^{*} as presented in Fig. 6.3. The voltage vectors in the plane are defined by a sequence of switching states as $\mathbf{v}_{x_j} = v_{rj} + \mathrm{j}v_{lj}$, where x represents the binary sequence $\{q_{gj}, q_{lj}, q_{sj}\}$. There are eight possible combinations of switching states q_{gj}, q_{lj}, and q_{sj} resulting in voltage vectors $\mathbf{v}_{x_j}$ that define triangular sectors ($K = 1, 2, .., 6$).

Consider that $\mathbf{v}_j^{*} = v_{rj}^{*} + \mathrm{j}v_{lj}^{*}$ represents the reference voltage vector to be generated by the converter which must be synthesized by the three closest voltage vectors to improve harmonic distortion. Since $\mathbf{v}_j^{*}$ is constant during the sampling period T and the three nearest voltage vectors are represented as $\mathbf{v}_{aj}$, $\mathbf{v}_{bj}$, and $\mathbf{v}_{cj}$, it can be written that

$$\mathbf{v}_j^{*} = \frac{t_{aj}}{T}\mathbf{v}_{aj} + \frac{t_{bj}}{T}\mathbf{v}_{bj} + \frac{t_{cj}}{T}\mathbf{v}_{cj}. \tag{6.12}$$

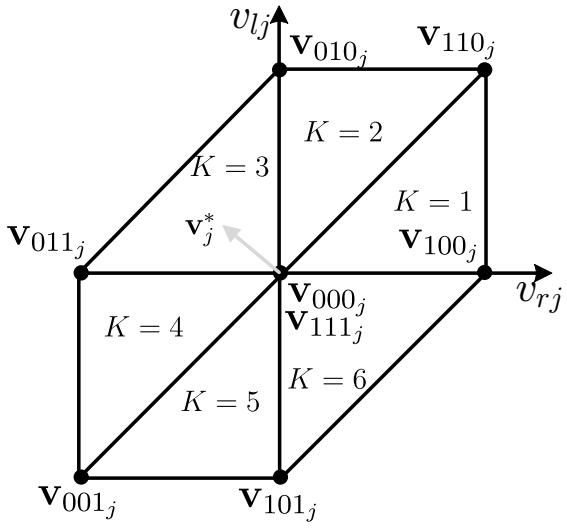
Decomposing (6.12) on the real (v_{rj}) and imaginary (v_{lj}) axis, it can be obtained that

$$\mathbf{v}_{rj}^{*} = \frac{t_{aj}}{T}\mathbf{v}_{arj} + \frac{t_{bj}}{T}\mathbf{v}_{brj} + \frac{t_{cj}}{T}\mathbf{v}_{crj}, \tag{6.13}$$

$$\mathbf{v}_{lj}^{*} = \frac{t_{aj}}{T}\mathbf{v}_{alj} + \frac{t_{bj}}{T}\mathbf{v}_{blj} + \frac{t_{cj}}{T}\mathbf{v}_{clj}, \tag{6.14}$$

where t_{aj}, t_{bj}, and t_{cj} are the application times of each voltage vector.

Figure 6.3 – Space-vector plan generated by the three-leg module.



6.3.2 Shunt Converter

Since the reference voltages across the shunt converter v_{hj}^* are defined from the current control, the desired reference pole voltage $v_{hj0_h}^*$ in each phase, as well as the reference voltage of the fourth leg are given by

$$v_{hj0_h}^* = v_{hj}^* + v_{l0_h}^*, \tag{6.15}$$

$$v_{h40_h}^* = v_{l0_h}^*, \tag{6.16}$$

The voltage $v_{l0_h}^*$ is calculated introducing the general apportioning factor. Once calculated $v_{hj0_h}^*$ and $v_{h40_h}^*$, the shunt converter is commanded using a triangle comparison PWM. The shunt converter may operate with lower switching frequency than the main converter in order to reduce switching losses.

6.3.3 Overall Control Strategy

Fig. 6.4(a) presents de control diagram of the proposed UPQC. The average dc-link voltages $[E_x = (E_1 + E_2 + E_3)/3]$ of the nine-leg converter is adjusted by a conventional PI controller. This controller provides the reference amplitude of the grid currents (I_{gj}^*). The phase shift θg is determined using a phase-locked loop (PLL) which allows synchronizing the instantaneous reference currents i_{gj}^* with the grid voltages (e_{gj}), ensuring a high power factor at the grid side. To control the grid currents, a proportional resonant (PR) controller receives the error $i_{gj} - i_{gj}^*$ and defines the reference voltage v_{gj}^*. The load voltage control is implemented using a PR controller. The instantaneous reference voltages e_{lj}^* are defined with the load voltage amplitude (E_{lj}^*) and load phase angle (θl). The PR block receives the error $e_{lj}^* - e_{lj}$ and provides the reference voltages v_{lj}^*.

In the studied system, the shunt converter provides balanced currents with reactive and harmonic compensation. In this way, the output currents of the nine-leg converter (i_{fj}) are controlled and the shared-leg currents (i_{sj}) can be minimized. The dc-link voltage of the shunt converter is regulated by a conventional PI compensator whose output is the reference amplitude of the nine-leg output reference current (I_{fj}^*). To minimize the currents in the shared legs, the instantaneous reference currents i_{fj}^* are synchronized with the grid voltage. The currents i_{fj} are controlled using a PR controller. This compensator generates the reference voltages v_{hj}^*.

6.3.4 Balancing of the three-leg module dc-link voltages

Additionally, to ensure the correct operation of the nine-leg converter, at least two dc-link voltages need to be regulated individually, since the third dc-link voltage

remains balanced by the average voltage control already explained. In this way, the voltages E_1 and E_2 are selected to be regulated individually. The reference common-mode voltage (v_{gs}^*), calculated by (6.11), establishes a degree of freedom defined by the general apportioning factor μ^*. In this way, this variable is used to control the delivered power in each three-leg module under unbalanced load and unbalanced voltage disturbances. Since the instantaneous power in each three-leg converter can be defined by $p_{3L_j} = v_{rj}^* i_{gj} - v_{lj}^* i_{lj}$, from (6.8), one can rewrite it as follow

$$p_{3L_j} = v_{gj}^* i_{gj} - v_{lj}^* i_{lj} + v_{gs}^* i_{gj} \tag{6.17}$$

The equation portion represented by $v_{gj}^* i_{gj} - v_{lj}^* i_{lj}$ is defined by the aforementioned control system detailed in Fig. 6.4(a). The remaining portion depends on the common-mode reference voltage. In this way, it can be defined, from (6.11), the instantaneous common-mode power as

$$p_{gs} = [\mu^* V_{max} + (1 - \mu^*) V_{min}] i_{gj} \tag{6.18}$$

As shown in Fig. 6.4(b), both dc-link voltages are controlled by a conventional PI controller whose output assigns a factor (μ_1 and μ_2) to the apportioning factor μ^*. Fig. 6.4(c) shows the balancing control taking into account the distribution of μ^*. To set the priority in which the dc links are charged or discharged, the highest absolute value of the currents i_{g1} and i_{g2} is considered, to produce the highest balancing control effectiveness in each phase.

6.4 Results

Simulations and experimental results are shown in a closed loop to confirm the proposed converter's feasibility and the design methodology's correctness. Simulation results have been performed through the software PSIM and experimental results were obtained using a platform consisting of power devices from SEMIKRON with dual module IGBT SKM50GB123 and dedicated gate drivers (SKH23). In addition, the converter was controlled by a Texas Instruments TMS320F228335 Digital Signal Processor (DSP) with plug-in devices and voltage and current sensors to measure the system variables. Table 6.1 presents the parameters used in the tests.

6.4.1 Simulation Results

Simulations were conducted to demonstrate the converter's performance under severe unbalanced load and under a grid voltage sag transient. In these tests, the following harmonics were included in the grid voltages: third (10%), fifth (5%), and seventh (2%) order

Table 6.1 – Parameters used in the tests.

Parameter		Value
Grid voltage	e_g	110 V rms 77 V rms
Load reference voltage	e_l^*	110 V rms
Switching frequency	f_s	10 kHz
Dc-link capacitor	C	2.2 mF
Dc-link voltage	E_j, E_h	160/320 V
Shunt inductance	L_g	5 mH
Load filter inductance	L_l	1 mH
Load filter capacitance	C_l	120 μH
Load filter dump resistance	R_l	10 Ω
Nonlinear load		
Phase 1	S_{l1} THD_{il}	0.77 kVA 40%
Phase 2	S_{l1} THD_{il}	0.45 kVA 53%
Phase 3	S_{l1} THD_{il}	0.45 kVA 53%

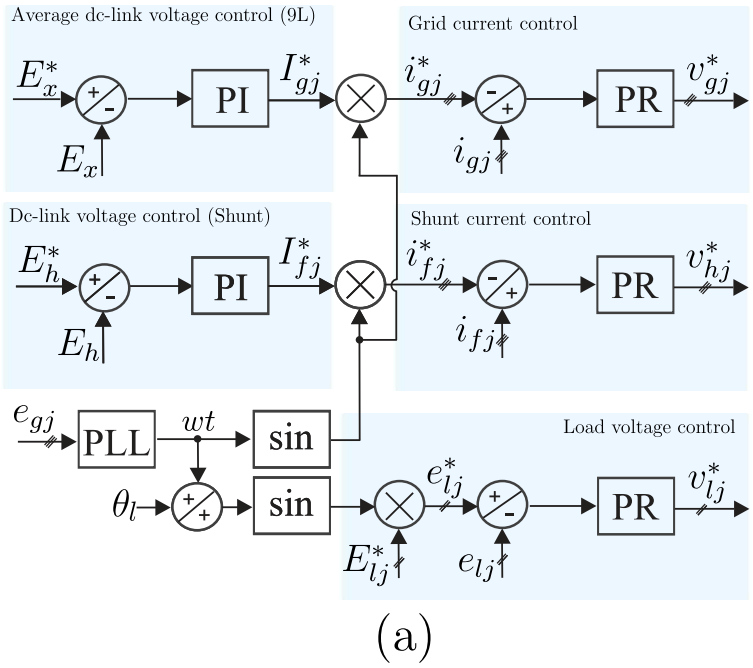
harmonics. In addition, an unbalanced nonlinear load based on single-phase uncontrolled rectifiers was considered. First, the operation under a severe unbalanced load is presented in Fig. 6.5. At t = 1 s, one phase suffers a severe load transient, which leads to a zero current. As can be seen, the grid currents remain balanced during the transient. In addition, the load voltages and the dc-link voltages of the nine-leg and shunt modules remain controlled. Fig. 6.6 shows operation with a symmetrical voltage sag of 30%. In the same way, the converter ensures operation with balanced grid current during disturbances and control of the load and dc-link voltages at their reference values.

6.4.2 Experimental Results

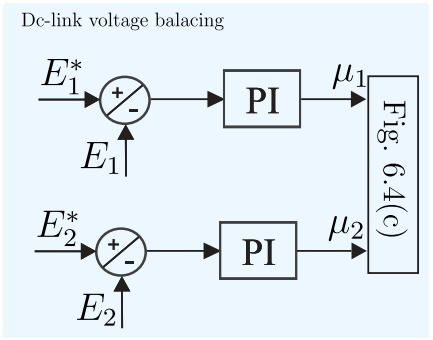
To verify the operation of the converter and its control strategy, a transient test with a severely unbalanced load was performed. Figures 6.7, 6.8, 6.9, 6.10, and 6.11 illustrate the main waveforms that demonstrate the proper functioning of the proposed converter during this transient. The results show that when the transient begins, the converter effectively maintains control over the load voltage (Fig. 6.9), dc-link voltages (Figs. 6.7 and 6.10), and grid current (Fig. 6.11), ensuring stable and balanced operation.

Next, a symmetrical voltage sag of 30% was applied to verify the operation of the series unit of the proposed converter. Fig. 6.12, 6.13 show the main waveforms to demonstrate the correct operation of the proposed converter at this transient. It can be seen that the dc-link voltages of the nine-leg converter are kept in their reference value, providing the load voltage control.

Figure 6.4 – Control system. (a) Control diagram to generate the shunt and series reference voltages. (b) Control diagram to generate the apportioning factors μ_1 and μ_2. (c) Flowchart for dc-link voltage balancing.



(a)



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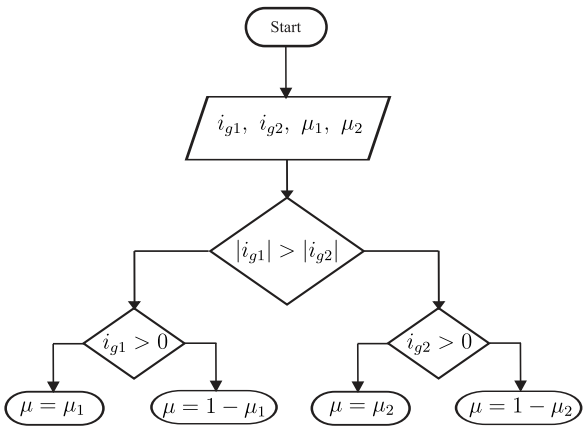


(c)

Figure 6.5 – Simulation results - Load phase opening transient.

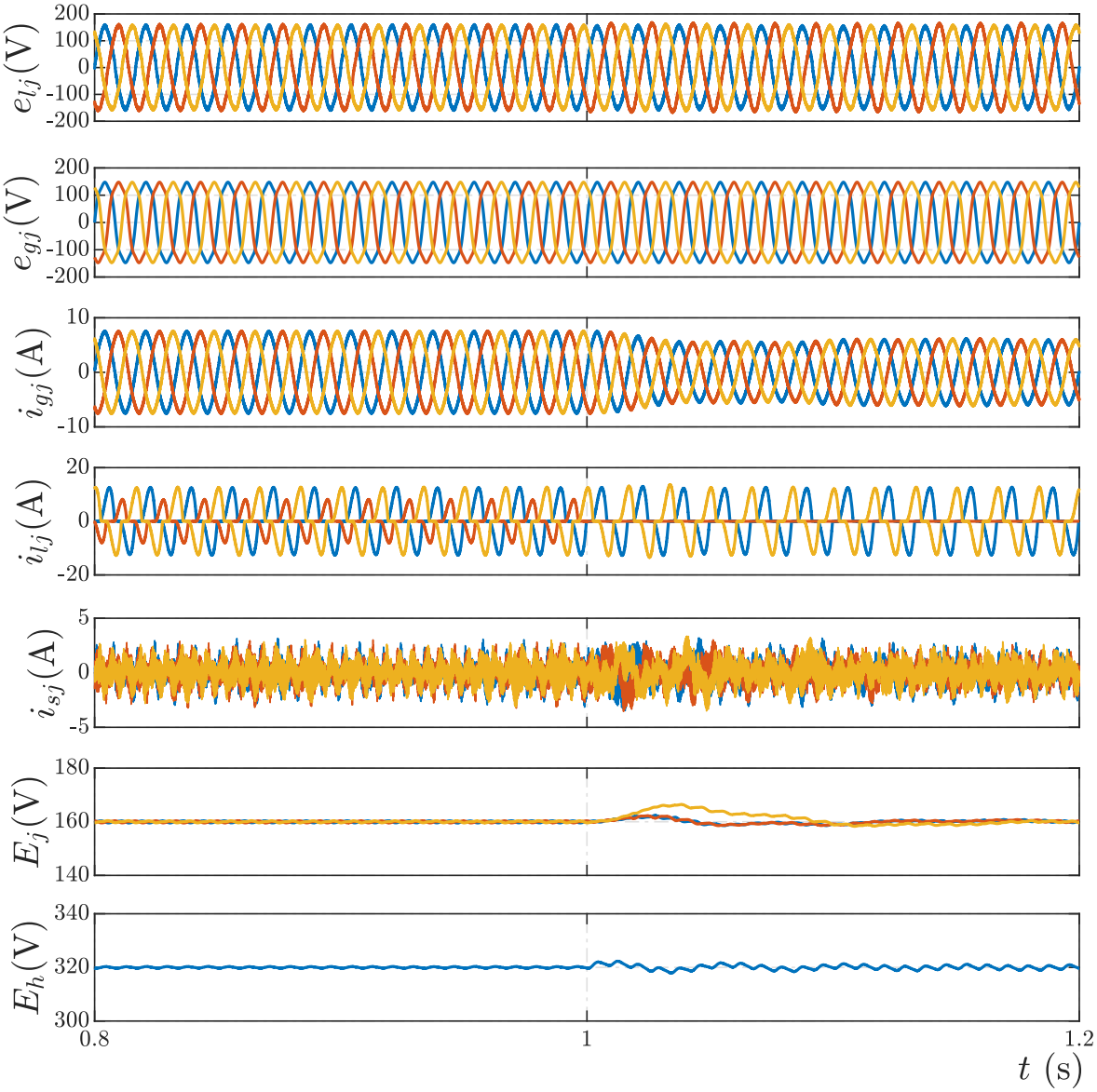


Figure 6.6 – Simulation results - Symmetrical voltage sag of 30%.

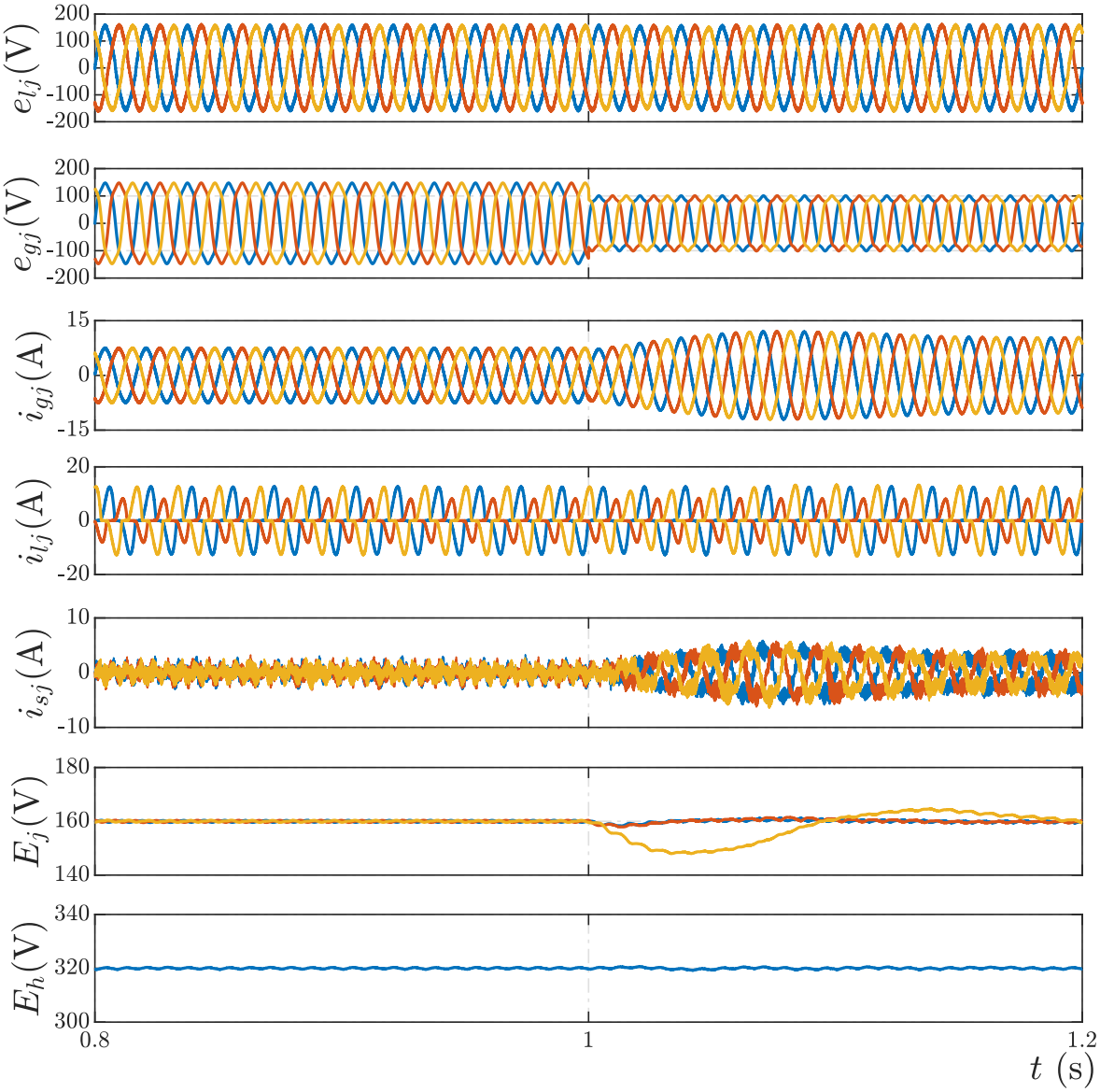
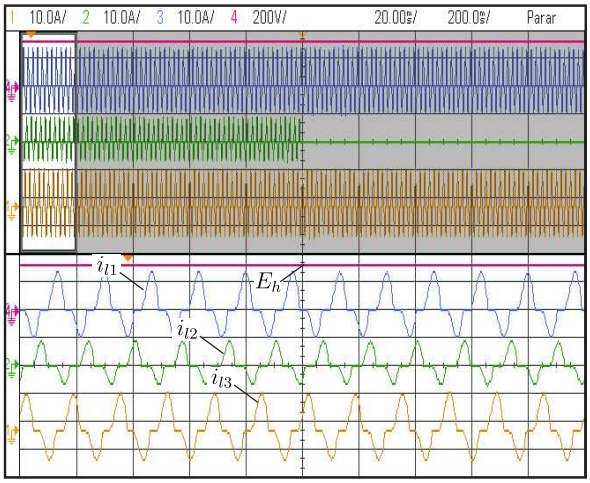
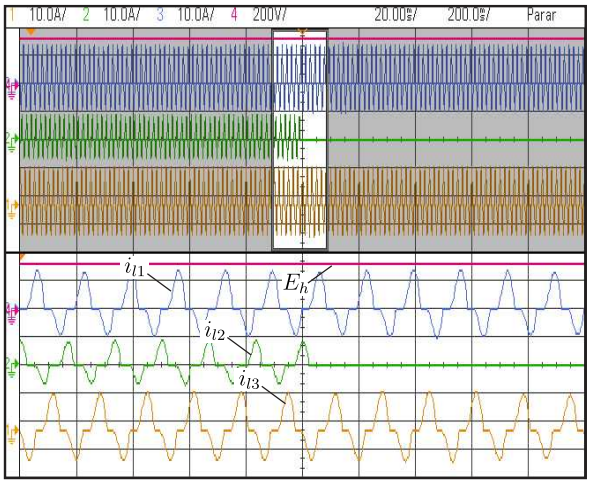


Figure 6.7 – Experimental results - Load phase opening transient. Load currents (i_{lj}) and dc-link voltage of the shunt converter (E_h) (a) before of the transient, (b) in the beginning of the transient, and (c) during the transient.



(a)



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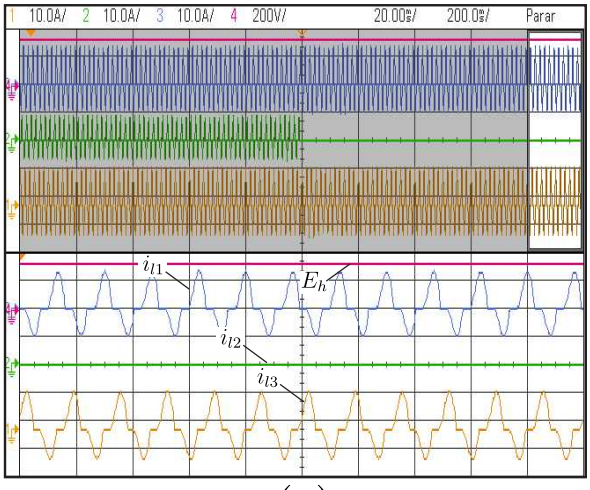
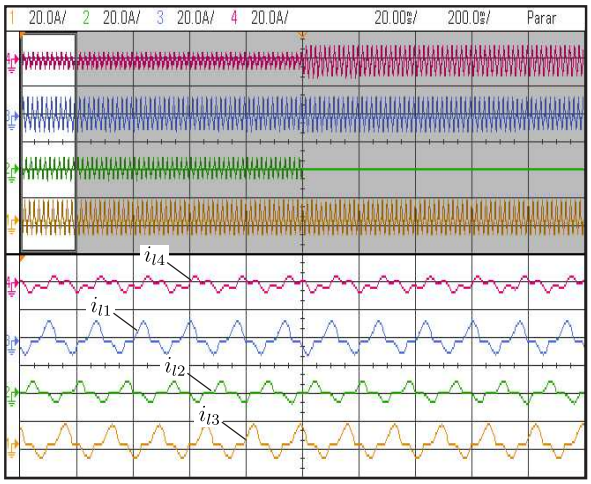
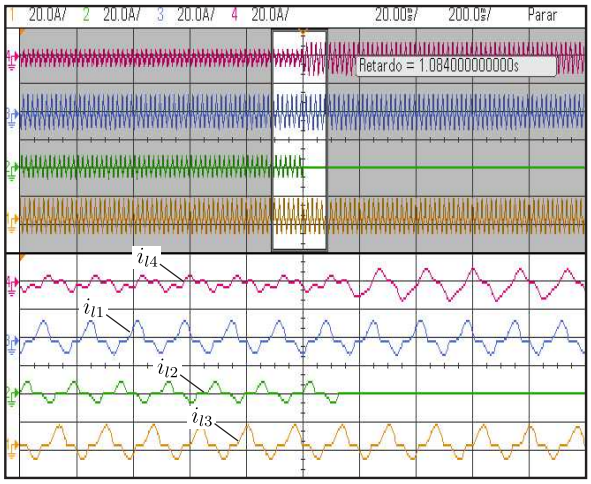


(c)

Figure 6.8 – Experimental results - Load phase opening transient. Load currents (i_{lj} and i_{l4}) (a) before of the transient, (b) in the beginning of the transient, and (c) during the transient.



(a)



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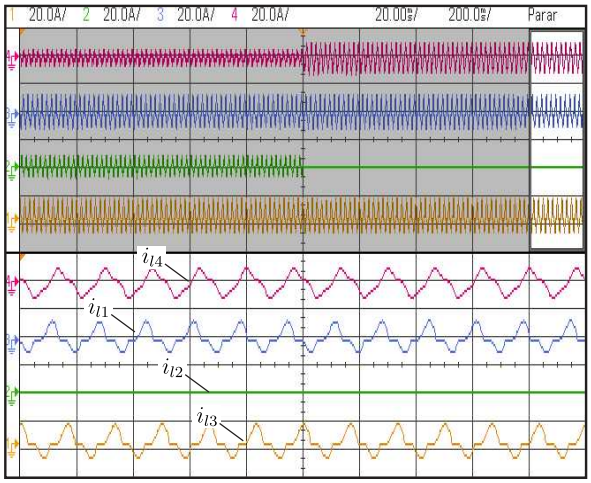
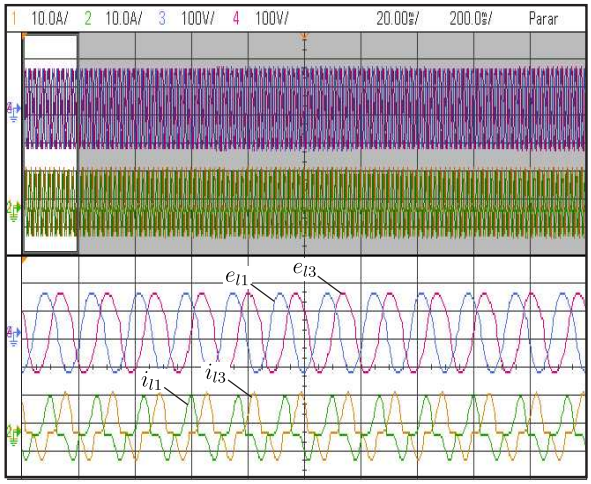
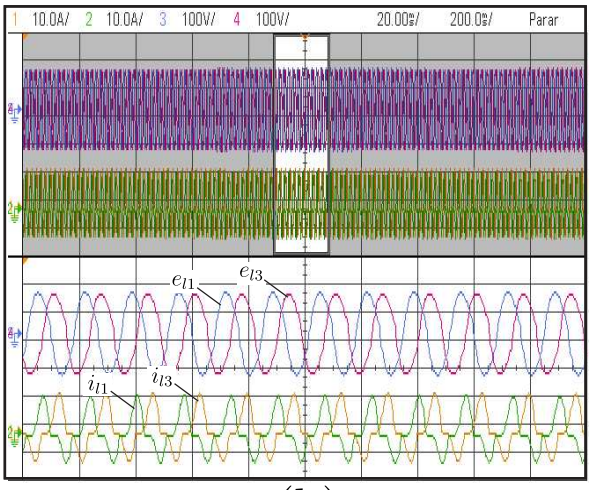


(c)

Figure 6.9 – Experimental results - Load phase opening transient. Load voltages (e_{l1} and e_{l3}) and Load currents (i_{l1} and i_{l3}) (a) before of the transient, (b) in the beginning of the transient, and (c) during the transient.



(a)



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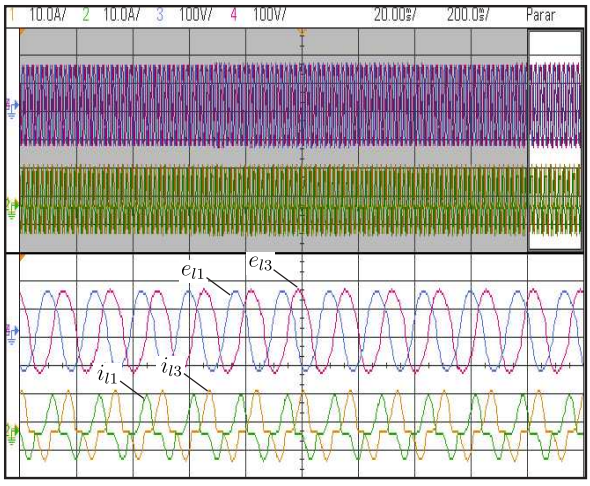
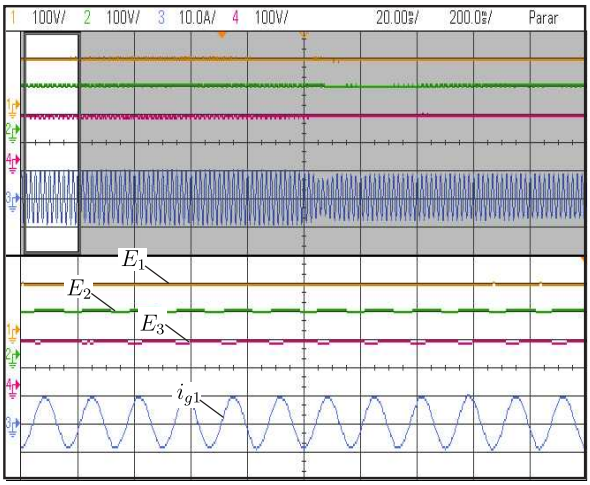
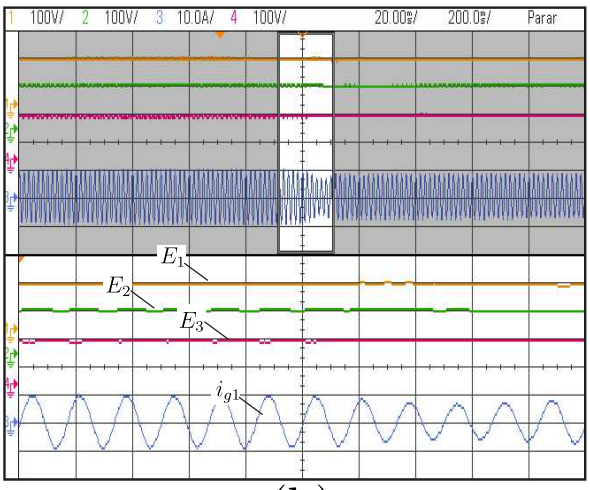


(c)

Figure 6.10 – Experimental results - Load phase opening transient. Dc-link voltages of the nine-leg converter (E_j) and grid current (i_{g1}) (a) before of the transient, (b) in the beginning of the transient, and (c) during the transient.



(a)



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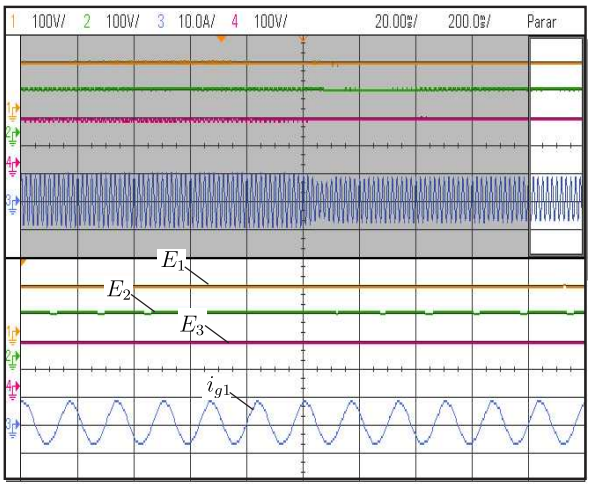
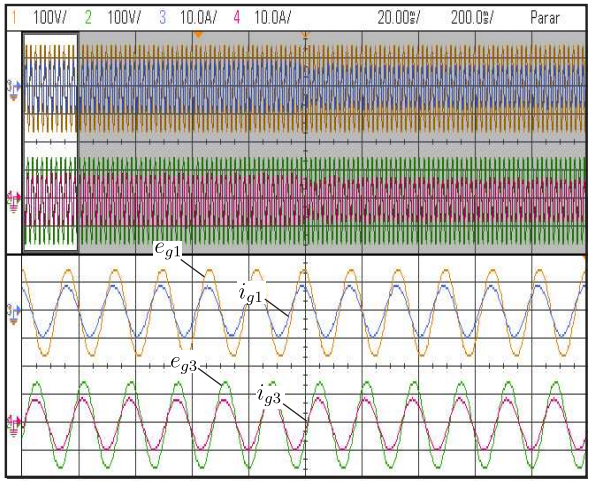
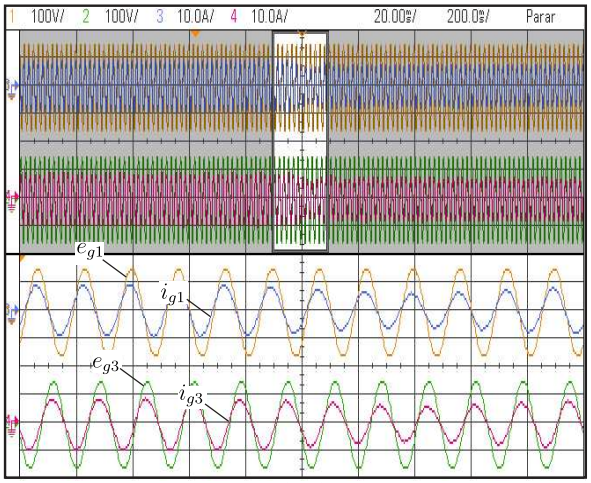


(c)

Figure 6.11 – Experimental results - Load phase opening transient. Grid voltages (e_{g1} and e_{g3}) and grid currents (i_{g1} and i_{g3}) (a) before of the transient, (b) in the beginning of the transient, and (c) during the transient.



(a)



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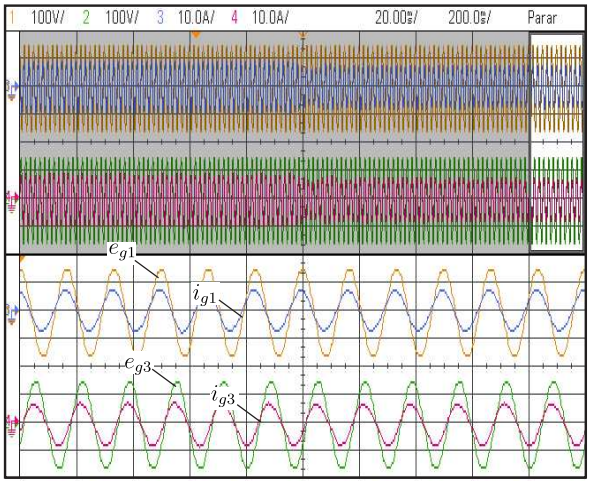
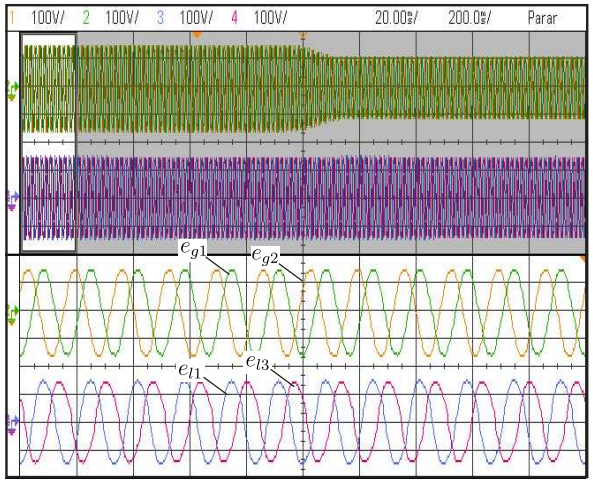
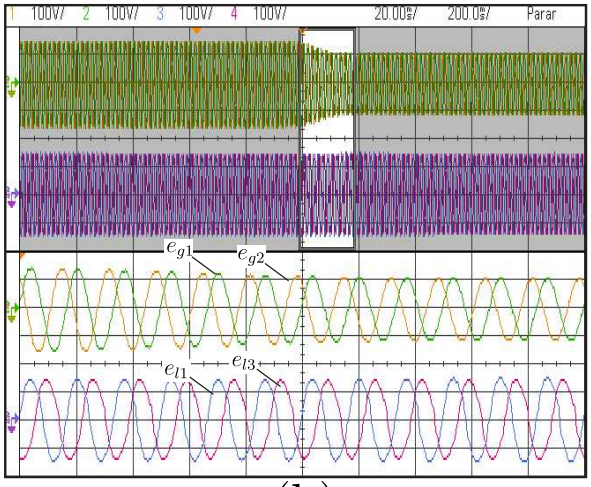


(c)

Figure 6.12 – Experimental results - Grid voltage sag transient. Grid voltages (e_{g1} and e_{g2}) and Load voltages (e_{l1} and e_{l3}) (a) before of the transient, (b) in the beginning of the transient, and (c) during the transient.



(a)



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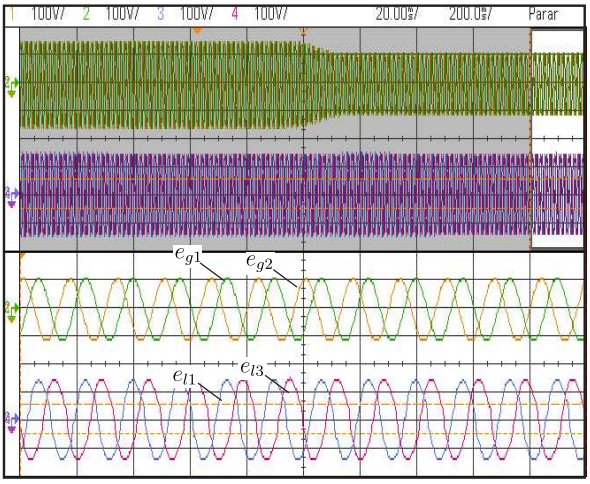
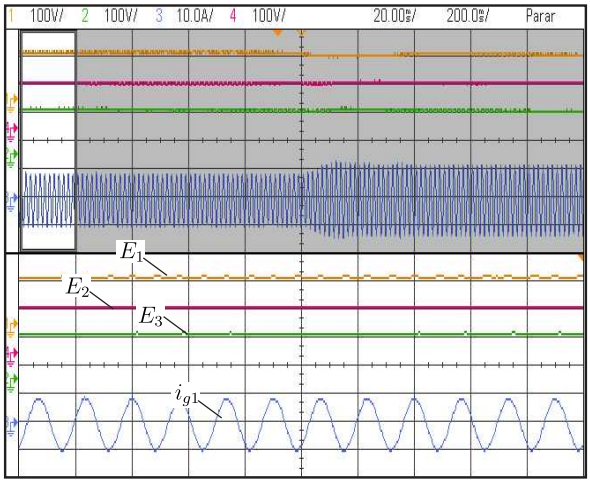


(c)

Figure 6.13 – Experimental results - Grid voltage sag transient. Dc-link voltages of the nine-leg converter (E_j) and grid current (i_{g1}) (a) before of the transient, (b) in the beginning of the transient, and (c) during the transient.



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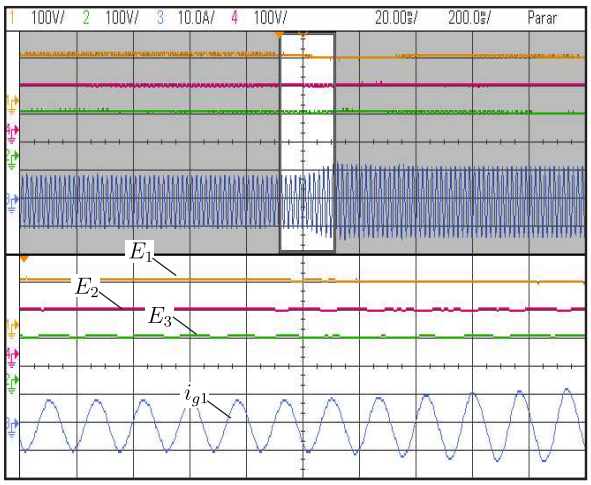

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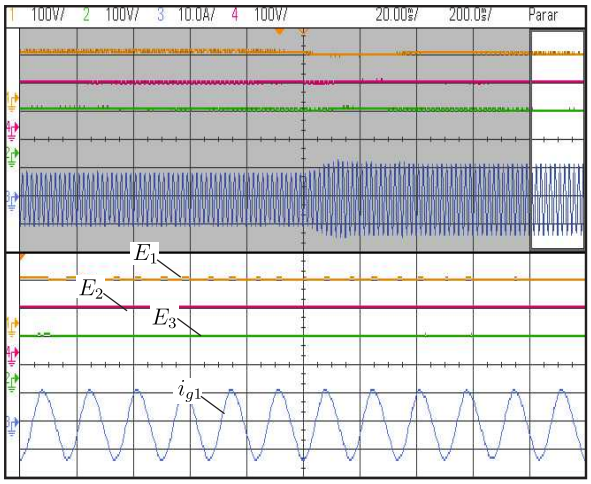


(c)

6.5 Semiconductor Losses and harmonic distortion

In this section, a further comparison between the proposed configuration and transformerless UPQC solutions in terms of semiconductor power losses and total harmonic distortion (THD) is provided. Simulations were performed to compare the proposed converter with the conventional solutions in (CHANG; CHANG; CHIANG, 2006) [see Fig. 1.17(b)] and (VENKATRAMAN; SELVAN, 2017) (see Fig. 1.18). To simplify the descriptions, these are here named respectively 9L and 6L. The parameters considered for these comparisons are summarized in Table 6.2. Also, for comparisons, the dc-link voltages of the main converter for the proposed converter are $E_j = 320$ V. The load is unbalanced, with one phase without any current, while the other two divide the total power. This unbalance require the converter 9L to increase its dc-link voltage to $E_j = 520$ V so that it is able to balance its dc-link voltages. Besides that, the converter 6L operates with dc-link voltages of 640 V.

Table 6.2 – Parameters used in comparative analysis.

Parameter	Value
Grid voltage e_g	220 Vrms
Reference load voltage v_l^*	220 Vrms
Dc-link voltage E_h	540 V
Grid and load fundamental frequency	60 Hz
Switching frequency of main converter	10 kHz
Switching frequency of shunt converter	2 kHz
Filter inductors	2.0 mH
Filter resitance	0.1 Ω
Filter capacitance C_l	18 mF
Load power	6 kW

The semiconductor losses were evaluated considering insulated gate bipolar transistor (IGBT) modules SKM50GB123D. The losses are composed by switching losses (P_{sw}) and conductions losses (P_{cd}), with $P_{loss} = P_{cd} + P_{sw}$. Results of semiconductor losses comparison are summarized in Fig. 6.14.

The quality of the waveforms of grid voltages and load currents are evaluated with the total harmonic distortion (THD), calculated by:

$$THD = \frac{100}{x_1}\sqrt{\sum_{u=2}^{N_u} x_u^2} \tag{6.19}$$

where x_1 is the amplitude of the fundamental component, x_u are the amplitudes of the harmonic components, u is the harmonic order and N_u is the number of considered harmonic components ($N_u = 1000$). Fig. 6.15 summarizes the harmonic distortion comparisons.

Considering the converters operating with the same switching frequency ($10kHz$), the proposed converter developed total converter losses 12% lower than the 9L and 16%

Figure 6.14 – Semiconductor losses. (a) Converters operating with $f_s = 10kHz$. (b) Converters operating with grid currents THD of 5%.

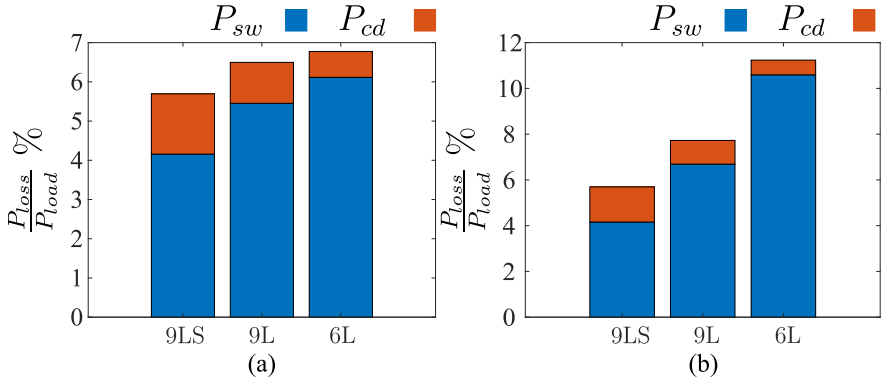
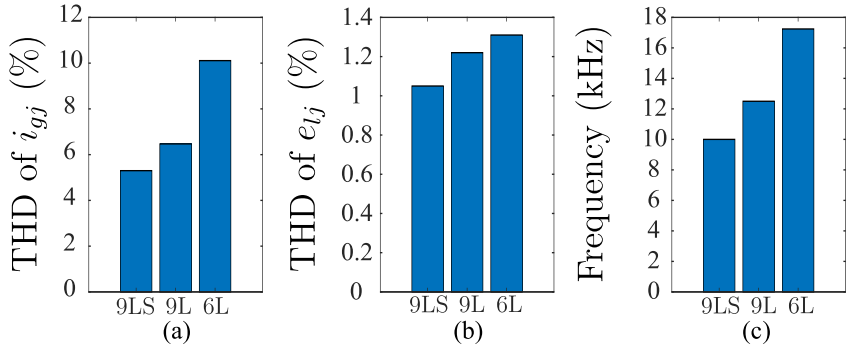


Figure 6.15 – (a) THD of grid currents $f_s = 10kHz$. (b) THD of load voltages $f_s = 10kHz$. (c) Switching frequency f_s for operation with grid currents THD of 5.3%.



lower than the 6L [Fig. 6.14(a)]. It also presented THD of grid currents 18% and 48% lower than the 9L and 6L, respectively [Fig. 6.15(a)]. Additionally, the proposed converter had THD of load voltages 15% lower than the 9L and 20% lower than the 6L [Fig. 6.15(b)]. In this scenario, the proposed converter had switching losses 24% and 32% lower than the 9L and 6L, respectively. On the other hand, the conventional converters 9L and 6L had conduction losses 32% and 57% lower the proposed one. This indicates that the proposed converter is competitive in scenarios where switching losses are dominant.

Since the proposed converter developed lower THD for the same switching frequency, it can operate with reduced frequency if compared with the conventional solutions. Then, Fig. 6.15(c) shows the frequencies of each converter for an operation with the same THD of grid currents (5.3%). To meet the same THD, the conventional 9L and 6L had to increase their switching frequency in 49% and 72%, respectively. In this new scenario, the proposed converter presented total semiconductor losses 26% and 49% lower than the 9L and 6L, respectively [Fig. 6.14(b)]. Also, it presented switching losses 38% and 61% lower than the 9L and 6L, respectively.

6.6 Conclusion

In this chapter it was proposed a three-phase transformerless unified power quality conditioner based on a nine-leg converter and a four-wire shunt converter. The proposed system can compensate voltage and current disturbance, as well as severe unbalances in the load. Simulations and experimental results were provided to validate the feasibility of the proposed 9LS-UPQC topology. In both analyzed scenarios, the proposed configuration has higher conduction losses than the conventional transformerless solutions (9L and 6L), as it has more power switches. On the other hand, it can be noticed that the proposed configuration achieves better results in terms of switching losses. This is possible because the 9L and 6L structures operate with a dc-link voltage value higher than the proposed configuration. In addition, the shunt converter in the proposed converter was set to operate with a switching frequency five times lower than 9L and 6L. In this way, the decrease in switching losses on the 9LS-UPQC converter compensates for the increase in the conduction losses. As a result, the proposed topology was able to achieve lower overall losses than conventional structures in both scenarios investigated. Compared to 9L and 6L converter, the proposed configuration addressed a reduction in the overall losses of 12% and 16%, respectively, in the first scenario and 26% and 49%, respectively, in the second scenario.

Chapter 7

Investigation of a Three-Phase Four-Wire Nine-Leg Converter Based on High-Frequency Link

7.1 Introduction

In the last decades, the increasing utilization of semiconductor and power electronics devices generated a great amount of nonlinear loads connected to the distribution systems. These loads inject harmonic components in the grid currents that also generate harmonic voltage components at the grid (KHOSRAVI et al., 2023), (MONTEIRO et al., 2024). Additionally, voltage sags can be caused by faults in the distribution system, starting large motors, turning on/off high-power loads (SILVA et al., 2020). In four-wire systems, unbalanced conditions may also be found, such as asymmetrical faults and poorly distributed nonlinear loads, leading to unbalanced grid voltages and currents, and neutral currents with excessively high amplitudes, requiring oversized neutral conductors and causing deteriorating of equipment such as transformers (GE et al., 2021). In this context, unified power quality conditioners (UPQCs) have gained relevance, due to their ability to mitigate disturbances of both grid currents and load voltages (HEENKENDA et al., 2023).

Conventional UPQC topologies consider the shunt and series converters connected to a single dc-link and the series converter is connected with line-frequency transformers [see Fig. 7.1(a)] (KHADKIKAR, 2012). However, line-frequency transformers are expensive components that often present high volume and weight. In this way, transformerless solutions have been proposed (VENKATRAMAN; SELVAN, 2017; ABDALAAL; HO, 2022; KWON; KWON; KWON, 2018; LU et al., 2016; SANTOS et al., 2014; MAIA et al., 2018).

The transformerless topologies of UPQCs also present drawbacks. If the injection transformer is removed from the conventional UPQC, and the single dc-link configuration is maintained, the resulting UPQC may present circulating currents, that require additional inductors and higher dc-link voltage to be controlled (SANTOS et al., 2014). Alternative topologies consider series and shunt converters with separate dc-links. For a three-phase configuration, each phase of the series converter is composed of a single-phase converter (VENKATRAMAN; SELVAN, 2017) [see Fig. 7.1(b)]. With separate dc-links, it is not possible to exchange power efficiently between shunt and series converters neither between different phases of the series filter. This feature makes topologies like the one in (VENKATRAMAN; SELVAN, 2017) to require dc sources during sag compensation, or utilize zero-energy compensation, which brings some drawbacks, such as limited compensation range, high dc-link voltage required and generation of phase jumps at load voltages (MEYER et al., 2008).

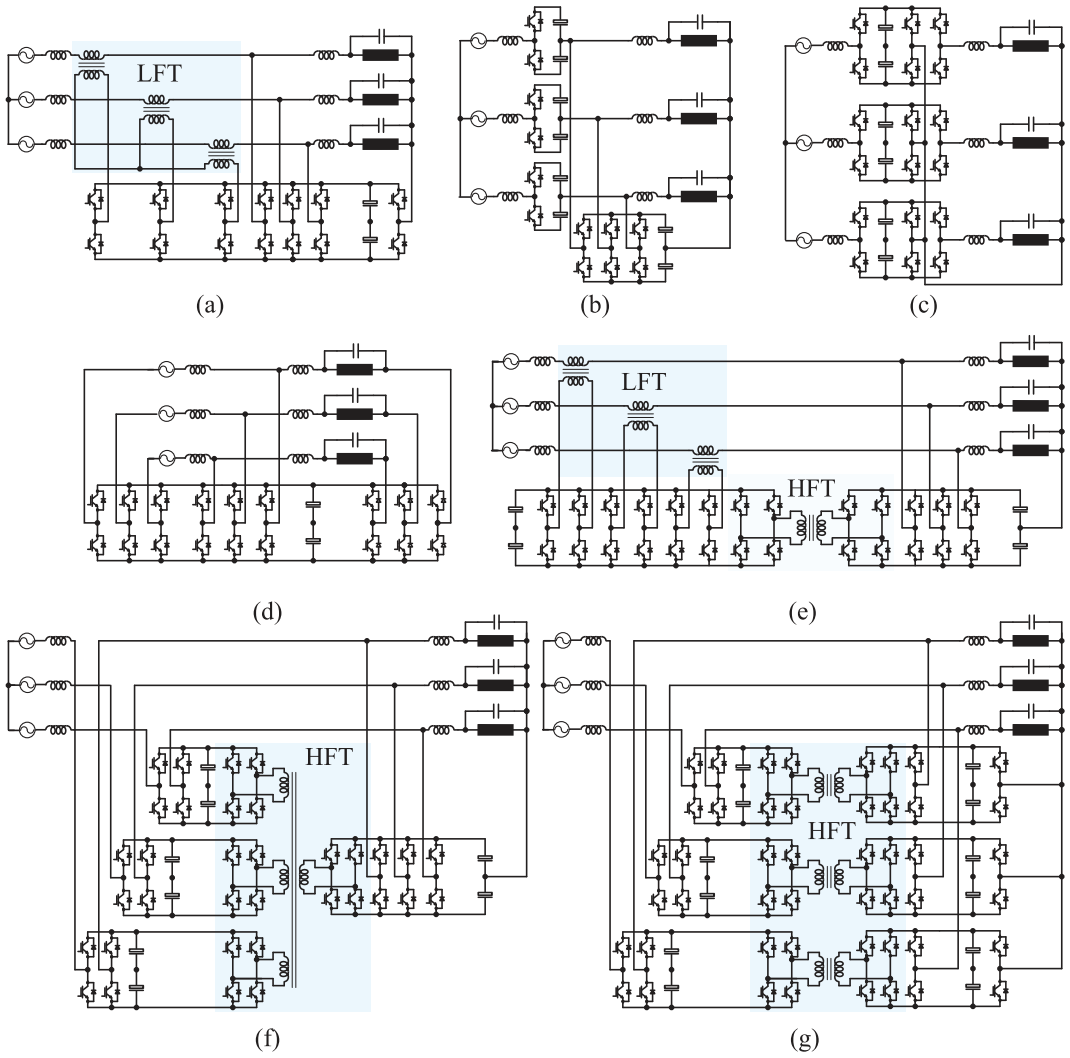
Other transformerless topologies consider one ac-dc-ac modules per phase (CHANG; CHANG; CHIANG, 2006; ABDALAAL; HO, 2022; KWON; KWON; KWON, 2018; LU et al., 2016). This type of UPQC presents limitations regarding power unbalances among different phases. For example, for the three-phase topology proposed in (CHANG; CHANG; CHIANG, 2006) and presented in Fig. 7.1(c), the maximum power unbalance allowed to guarantee control of dc-links is ±30% (MAIA et al., 2018). To address with this constraint, a topology was proposed in (MAIA et al., 2018) with a single dc-link [see Fig. 7.1(d)]. However, it requires an open-ended connection at both grid and load. An open-ended grid is not usually used, thus to obtain one, it would require additional line-frequency transformers, that if were taken into account, would increase highly the size and cost of the converter.

A commonly applied solution in machine drives (PEREDA; DIXON, 2011; Diab et al., 2018; Pereda; Dixon, 2012), battery energy storage systems (BESS) (WANG et al., 2023b; ZHENG et al., 2021), solid-state transformers (PEI et al., 2023; ZHU et al., 2023; PAN et al., 2023a), and other applications (MAJMUNOVIć et al., 2022; PAN et al., 2023b) to connect dc-links of different converter modules is the use of dc-dc converters with high-frequency transformers. This approach minimizes the system size by replacing line-frequency transformers with high-frequency ones. Similar techniques have been implemented in active power filters, feeding dynamic voltage restorers (DVRs) (Jimichi; Fujita; Akagi, 2011; Savrun et al., 2020) or connecting different dc-links of UPQCs (TONGZHEN; JIN, 2014; KOROGLU et al., 2020; HAN et al., 2021) [see Fig. 7.1(e-g)]. For application as UPQC, generally bidirectional dc-dc converters are required and different topologies may be applied (HONG et al., 2023; LI et al., 2023; LIU et al., 2023).

In this context, a three-phase four-wire converter composed by a ac-dc-ac three-leg module in each phase and a bidirectional three-port dc-dc converter isolated with a

three-winding high-frequency transformer (see Fig. 7.2) is investigated in this chapter. The studied configuration consists in connecting the three dc-links of the three-phase converter introduced in (CHANG; CHANG; CHIANG, 2006) with a triple active-bridge (TAB) dc-dc converter (FELINTO; JACOBINA, 2020). This connection allows the the converter to operate with unbalanced power conditions, because the TAB is able to redistribute power among the converter phases. Converter model is provided, as well as pulse-width modulation, control strategy, and a comparative analysis. Experimental results are presented for validation purposes under severe unbalanced conditions. Compared with conventional solutions, the investigated converter offers advantages such as not requiring line-frequency transformers. In addition, compared to solutions that use high-frequency links, it reaches better results in terms of harmonic distortion and power losses.

Figure 7.1 – Conventional UPQC solutions considered in the comparative analyses. (a) Conventional UPQC with single dc-link and LFT (KHADKIKAR, 2012) (7LFT). (b) Transformerless UPQC with separate shunt and series half-bridge modules (VENKATRAMAN; SELVAN, 2017) (6L-OPEN). (c) Transformerless UPQC based on three-leg modules (CHANG; CHANG; CHIANG, 2006) (9L). (d) Transformerless nine-leg UPQC with single dc-link (MAIA et al., 2018) (9LD). (e) UPQC solution endowed by both LFT and dc-dc converters (KOROGLU et al., 2020) (13LHFT). (f) UPQC topology based on quadruple-active-bridge DC-DC converter (HAN et al., 2021) (17HFT). (g) UPQC solution based on series/shunt H-bridges and DC-DC converters (24HFT) (TONGZHEN; JIN, 2014).



7.2 Converter Model

The converter equations on time domain can be derived from the equivalent circuits presented in Fig. 7.3 applying Kirchhoff's laws. Henceforward, $j = \{1, 2, 3\}$, representing the three phases of the system.

The dynamic behavior of grid currents and load voltages are defined by (7.1) and (7.2), respectively, where e_{gj} are the grid voltages, i_{gj} are the grid currents, R_g and L_g are the resistance and inductance of the filter inductor and v_{gj} are the converter voltages at grid side, defined by (7.3). The load voltages are defined by (7.4).

$$v_{gj} = e_{gj} - R_g i_{gj} - L_g \frac{di_{gj}}{dt}, \tag{7.1}$$

$$v_{lj} = e_{lj} + R_l i_{Lj} + L_l \frac{di_{Lj}}{dt} + R_l C_l \frac{de_{lj}}{dt} + L_l C_l \frac{d^2 e_{lj}}{dt^2}, \tag{7.2}$$

$$v_{gj} = v_{rj} - v_{gs}, \tag{7.3}$$

$$v_{lj} = v_{lj0} - v_{sj0}. \tag{7.4}$$

The voltage v_{rj} and the common-mode voltage v_{gs} is defined, respectively, by (7.5) (7.6). Furthermore, considering $k = \{g, l, s, t, h\}$ and the switch states q_{kj} represented as binary variables, where $q_{kj} = 1$ indicates the switch is on and $q_{kj} = 0$ indicates it is off, the pole voltages are expressed by (7.7). v_{Cj} are the dc-link voltages.

$$v_{rj} = v_{gj0} - v_{sj0}, \tag{7.5}$$

$$v_{gs} = \frac{1}{3}(v_{r1} + v_{r2} + v_{r3}), \tag{7.6}$$

$$v_{aj0} = \frac{v_{Cj}}{2}(2q_{aj} - 1). \tag{7.7}$$

The grid currents (i_{gj}), shunt compensation currents (i_{sj}), load currents (i_{lj}), and load neutral current (i_{l0}) are related by

$$i_{gj} - i_{lj} - i_{sj} = 0, \tag{7.8}$$

$$i_{l0} = i_{l1} + i_{l2} + i_{l3}. \tag{7.9}$$

Figure 7.2 – 9LHF-UPQC configuration.

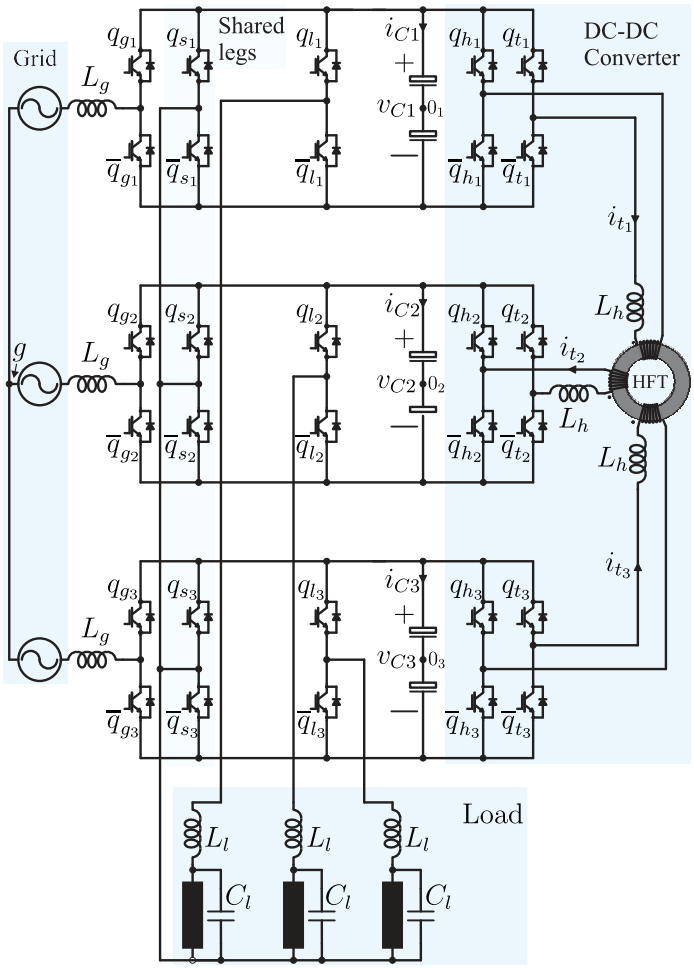
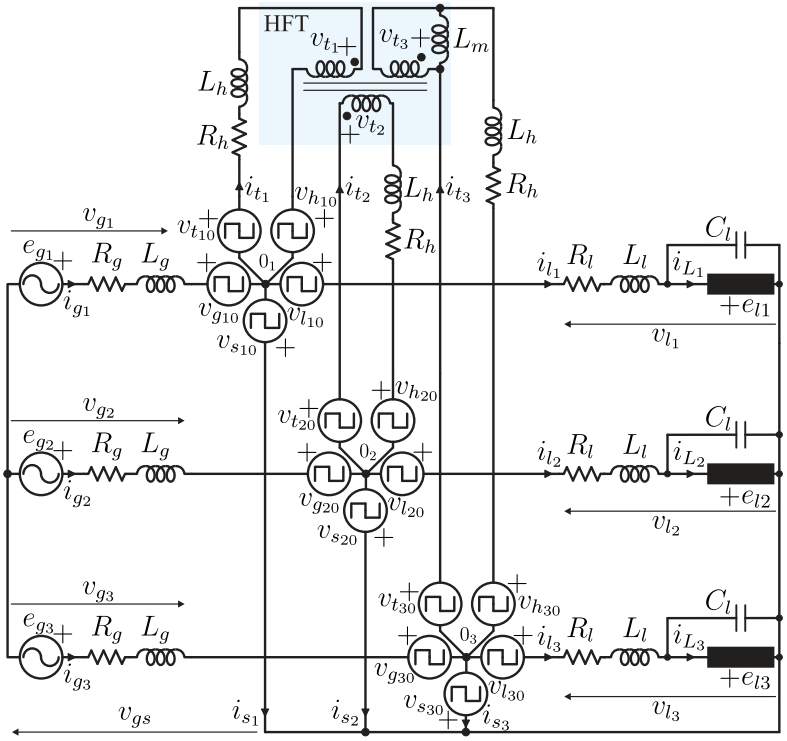


Figure 7.3 – Equivalent circuit of the 9LHF-UPQC configuration.



The current in each dc-link i_{Cj} is determined by (7.10), where q_{tj} and q_{hj} are the dc-dc converter switches and i_{tj} are the currents of the high-frequency transformer.

$$i_{Cj} = i_{gj}q_{gj} - i_{sj}q_{sj} - i_{lj}q_{lj} + (q_{tj} - q_{hj})i_{tj} = C_{dc}\frac{dv_{Cj}}{dt}, \tag{7.10}$$

where C_{dc} is the dc-link capacitance.

The dynamic behavior of the transformer currents is determined by (7.11), where v_{tj} are the transformer voltages, L_h is the inductor series connected to the transformer, with inner resistance R_h. In addition, L_m is the magnetizing inductance of the high-frequency transformer. The turns ratio of the transformer is always 1:1:1 due to the symmetry of the system, then (7.12) is derived.

$$v_{tj0} - v_{hj0} - v_{tj} = R_h i_{tj} + L_h\frac{di_{tj}}{dt}, \tag{7.11}$$

$$v_{t1} = v_{t2} = v_{t3} = L_m\frac{di_m}{dt}. \tag{7.12}$$

7.3 Pulse-Width Modulation

The PWM strategy applied to the nine-leg converter is the same described in the previous chapter for the 9LS-UPQC. Fig. 7.4 presents the space-vector diagram with eight switching vectors generated by each three-leg module, divided in six triangular sectors (I - VI). The duty cycles for each switch are calculated according to Table 7.1. This table also indicates the location of each sector, the chosen vector sequence and which switch remains clamped in each sector. To obtain the vector sequences and equations presented in Table 7.1, first, the switch to be clamped is chosen. For this switch, the reference pole (v^*_{kj0}) voltage is $0.5v^*_C$ for $q_{kj} = 1.0$ and $-0.5v^*_C$ for $q_{kj} = 0.0$. The remaining two pole voltages of the same phase are calculated by (7.13)-(7.14), obtained from (7.4) and (7.5).

$$v^*_{lj} = v^*_{lj0} - v^*_{sj0}, \tag{7.13}$$

$$v^*_{rj} = v^*_{gj0} - v^*_{sj0}. \tag{7.14}$$

The duty cycles (d^*_{aj}) are calculated with (7.4), obtained from (7.7)

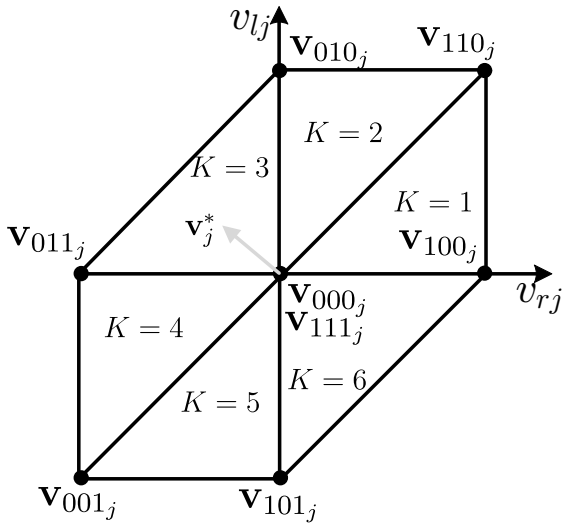
$$d^*_{aj} = \frac{v^*_{aj0}}{v^*_C} + 0.5. \tag{7.15}$$

Finally, the duty-cycles are compared with a triangular carrier.

For the ac side, the switching frequencies are equal and all carriers operate with the same phase. For the dc-side, it is considered $f_h = f_t$ and the reference pole voltages are

$$v^*_{hj0} = v^*_{tj0} = 0, \tag{7.16}$$

Figure 7.4 – Space vector PWM diagram.



in addition, the carriers $v_{\Delta hj}$ and $v_{\Delta tj}$ are phase-shifted by 180°, such that the switches q_{hj} and q_{tj} operate complementarily ($q_{tj} = 1 - q_{hj}$), generating square voltages in the output of the h-bridges.

Table 7.1 – Location of the triangular sectors of the SVPWM, calculation of duty-cycles and resulting vector sequence.

Sector	$\mathbf{v}_j^1 \Rightarrow \mathbf{v}_j^2 \Rightarrow \mathbf{v}_j^3$	d^*_{gj0}	d^*_{lj0}	d^*_{sj0}	d^*_{tj}	d^*_{hj}
I	$\mathbf{v}_4 \Rightarrow \mathbf{v}_6 \Rightarrow \mathbf{v}_7$	1.0	$\frac{v^*_{lj}-v_{rj^*}}{v^*_C} + 1.0$	$1.0 - \frac{v_{rj^*}}{v^*_C}$	0.5	0.5
II	$\mathbf{v}_2 \Rightarrow \mathbf{v}_6 \Rightarrow \mathbf{v}_7$	$\frac{v^*_{rj}-v_{lj^*}}{v^*_C} + 1.0$	1.0	$1.0 - \frac{v_{lj^*}}{v^*_C}$	0.5	0.5
III	$\mathbf{v}_2 \Rightarrow \mathbf{v}_3 \Rightarrow \mathbf{v}_7$	$\frac{v^*_{rj}-v_{lj^*}}{v^*_C} + 1.0$	1.0	$1.0 - \frac{v_{lj^*}}{v^*_C}$	0.5	0.5
IV	$\mathbf{v}_0 \Rightarrow \mathbf{v}_1 \Rightarrow \mathbf{v}_3$	0.0	$\frac{v^*_{lj}-v_{rj^*}}{v^*_C}$	$-\frac{v_{rj^*}}{v^*_C}$	0.5	0.5
V	$\mathbf{v}_0 \Rightarrow \mathbf{v}_1 \Rightarrow \mathbf{v}_5$	$\frac{v^*_{rj}-v_{lj^*}}{v^*_C}$	0.0	$-\frac{v_{lj^*}}{v^*_C}$	0.5	0.5
VI	$\mathbf{v}_4 \Rightarrow \mathbf{v}_5 \Rightarrow \mathbf{v}_7$	1.0	$\frac{v^*_{lj}-v_{rj^*}}{v^*_C} + 1.0$	$1.0 - \frac{v_{rj^*}}{v^*_C}$	0.5	0.5

7.4 Control Strategy

Fig. 7.5 presents a block diagram of the control strategy. The average dc-link voltage error ($v^*_C - \bar{v}_C$) is evaluated by a conventional PI controller and returns the amplitude of the reference currents (I^*_g), where $\bar{v}_C = \frac{v_{C1}+v_{C2}+v_{C3}}{3}$. The sinusoidal grid reference currents (i^*_{gi}) are generated with the amplitude I^*_g and synchronized with the positive-sequence component of the grid voltages with a phase-locked loop (PLL) that captures the phase of positive sequence component of the grid voltage (θ_g). Resonant controllers evaluate the current errors ($i_{gi} - i^*_{gi}$) and return the converter reference voltages v^*_{g1}, v^*_{g2}, and v^*_{g3}. The load voltage control is also implemented using a resonant controller. The resonant

controller sets the series reference voltage, v_{lj}^*, taking into account the amplitude of the load reference voltage E_{lj}^* and its phase angle.

Regarding the control of the dc-dc converter based on high-frequency transformer, here it is considered a phase-shift approach. The control of the power flux in the TAB converter is then made by phase-shifting the carriers of each phase. In this way, the carriers $v_{\Delta h1}$, $v_{\Delta h2}$ and $v_{\Delta h3}$, respectively, have phases of 0°, ϕ_2 and ϕ_3. The phases ϕ_2 and ϕ_3 are determined by the control strategy. Two PI controllers, $k = \{2, 3\}$ evaluate the voltage errors $v_{Ck} - v_{C1}$, and return the phases ϕ_k in degrees ($-90° < \phi_k < 90°$). Fig. 7.6 illustrates the operation stages of the dc-dc converter for a specific set of angles ϕ_k.

Figure 7.5 – Control strategy diagram.

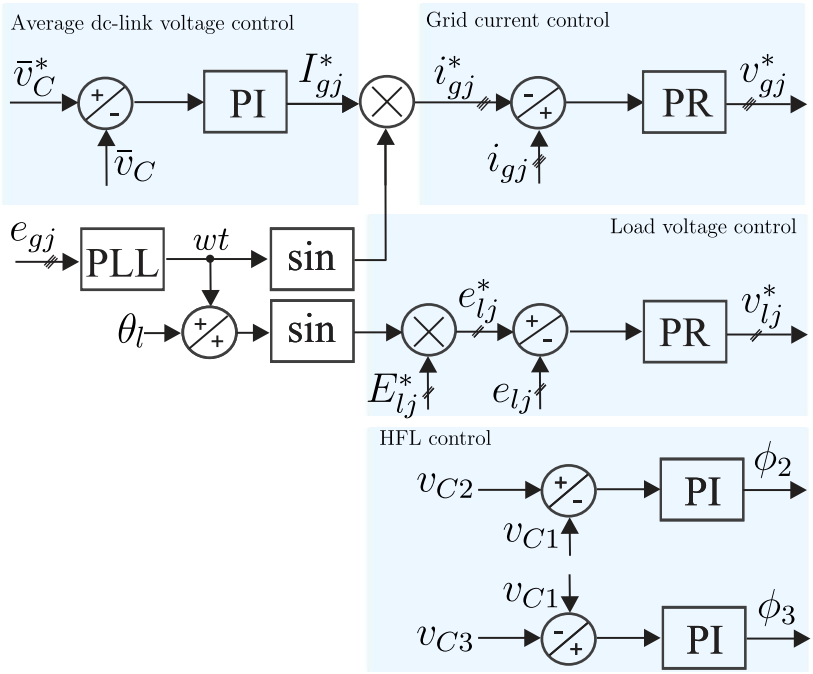
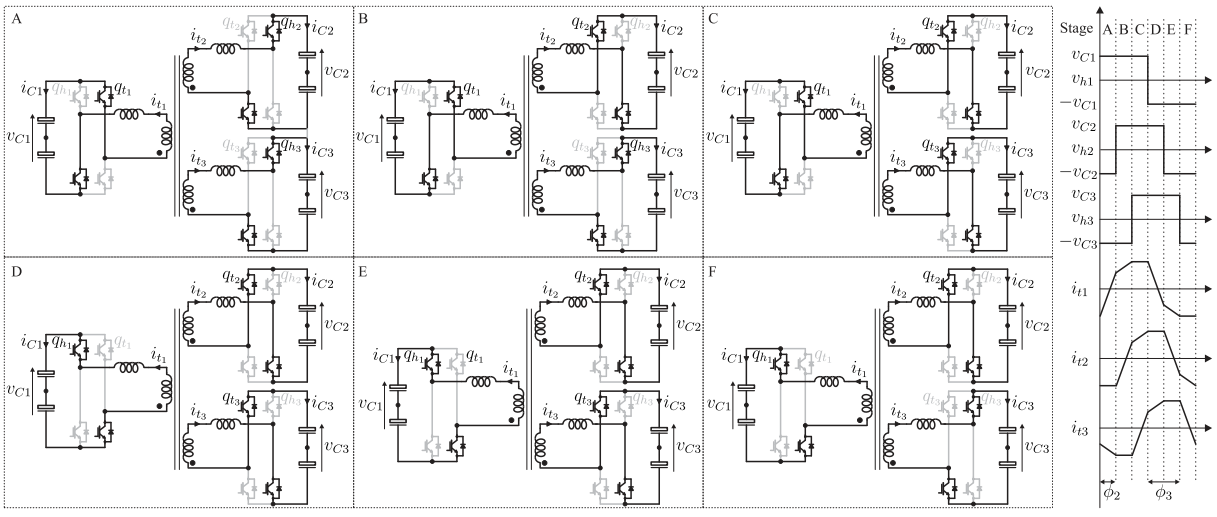


Figure 7.6 – Operation stages of the DC-DC converter for a specific set of angles ϕ_k.



7.4.1 Dc-link Voltage Requirements

From (7.13) and (7.14), considering that $-\frac{v_C^*}{2} \leq v_{kj0}^* \leq \frac{v_C^*}{2}$, the following inequalities can be derived:

$$v_C^* \geq |v_{rj}^*| \tag{7.17}$$

$$v_C^* \geq |v_{lj}^*| \tag{7.18}$$

Also, subtracting two phases of (7.14), it leads to $v_{g1}^* - v_{g2}^* = v_{g10}^* - v_{s10}^* - v_{g20}^* + v_{s20}^*$, which leads to

$$2v_C^* \geq |v_{g1}^* - v_{g2}^*| \tag{7.19}$$

and similarly, to

$$2v_C^* \geq |v_{g1}^* - v_{g3}^*| \tag{7.20}$$

Also, subtracting (7.13) from (7.14), it leads to $v_{rj}^* - v_{lj}^* = v_{gj0}^* - v_{lj0}^*$. From this, the following inequality is found:

$$v_C^* \geq |v_{rj}^* - v_{lj}^*| \tag{7.21}$$

The dc-link voltage and converter references must satisfy this five inequalities in order for the voltages to be properly generated.

From (7.21), it is possible to infer that the angle between grid and load voltages (δ_{gl}) also influences the choice of the dc-link voltage. One way to verify if a certain angle provokes the need to increase the dc-link voltage is drawing the locus of the reference vector $\mathbf{V_j^*}$ inside the space-vector diagram, as depicted in Fig. 7.7(b). It has been verified that the maximum angle that allows a dc-link voltage minimization is $\delta_{gl} = 60°$. For higher angles, the locus of the reference vector would exceed the space-vector diagram and what would indicate that the dc-link voltage should be increased. However, this angle limitation is easily satisfied in the converter operation. If this condition is satisfied, the minimum dc-link voltage is

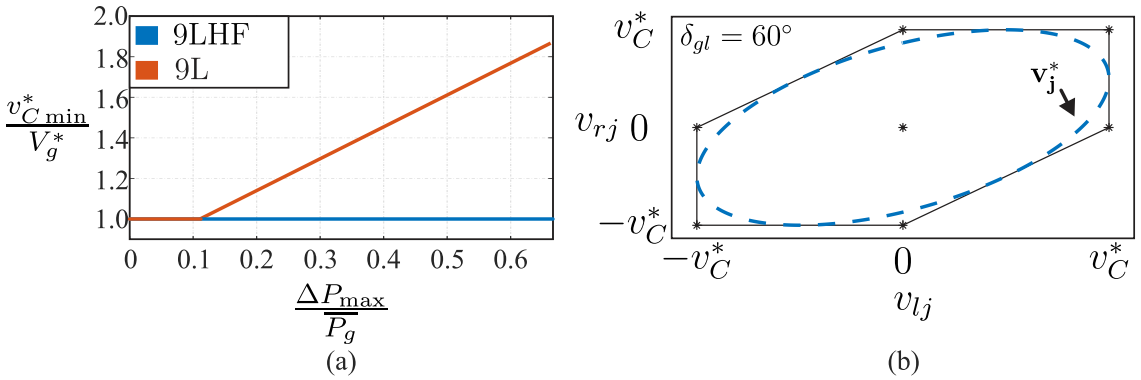
$$v_{C_{\min}}^* = \max\left(V_l^*, \frac{\sqrt{3}}{2}V_g^*\right) \tag{7.22}$$

where V_g^* is the amplitude of the converter grid-side reference voltages v_{gj}^*.

Other aspect that may influence the minimum dc-link voltage is the power unbalance between phases. The converter firstly proposed (CHANG; CHANG; CHIANG, 2006) and depicted in Fig. 7.1(c), consists of the investigated in this work without the dc-dc converter to connect the dc-links. This conventional converter has a limitation when it comes to operating in scenarios with unbalanced power distribution among phases. For higher power unbalances, it requires a higher dc-link voltage for the dc-link voltage control to occur. The investigated structure does not have this limitation. For any level of power unbalance, the dc-link voltage can be minimized. Fig. 7.7(a) shows a minimum dc-link comparison

between both configurations, where $\Delta P_{\max}$ is the maximum power difference relative to the average active power of the three phases. It can be seen that for power unbalances of 60%, the conventional topology needs to increase its dc-link voltage by almost 80% while the 9LHF-UPQC may operate with minimum dc-link voltage.

Figure 7.7 – (a) Comparison of minimum DC-link voltage with and without the high-frequency link as a function of the power unbalance among phases. (b) Maximum phase angle for minimum DC-link voltage.



7.5 Results

To verify the feasibility of the investigated system, simulations, and experimental results were done for validation purposes under severe unbalanced conditions. The experimental results were performed with SEMIKRON IGBT modules SKM50GB123D and drivers SKHI23. Control and PWM modulation were accomplished by digital signal processor (DSP) TMS320F28335. The parameters considered are listed in Table 7.2.

7.5.1 Simulation Results

Fig. 7.8 shows simulation results during a transient caused by a reduction of 33% in the nominal load power. Fig. 14(a-c) depicts the balanced grid voltages, dc-link voltages, and load currents. As can be seen, the dc-link voltages remain controlled before and after the transient. Fig. 7.8(d-f) depicts the grid currents during the transient. The decrease in the load currents decrease the grid currents, ensuring the dc-link voltage control. Fig. 7.8(g-i) present the load voltage behavior. As can be seen, the load voltages keep controlled. Fig. 7.9 shows simulation results during a transient caused by a reduction of 66% in the nominal load power. In the same way, the investigated converter ensures the grid currents control, which allows dc-link voltages regulation in these reference values. In addition, the load voltages remain controlled.

Fig. 7.10 and 7.11 show simulation results during a transient caused by a single-phase and two-phase fault, respectively. The investigated converter ensures grid current control, dc-link regulation, and load voltage compensation in both scenarios.

Table 7.2 – Parameters considered for simulation and experimental results

Parameter		Value
Comparative Analysis Parameters		
Grid voltage amplitude	E_g	311 V
Reference load voltage amplitude	V_l^*	311 V
Grid and load fundamental frequency	f_o	60 Hz
Dc-link voltages	v_{Cj}	320 V
Grid filter inductors	L_g	3 mH
Load filter inductors	L_l	2 mH
Load filter capacitors	C_l	45 μF
Dc-link capacitors	C_{dc}	4.5 mF
PWM frequency	f_a	10 kHz
Load Power	P_l	6 kW
Simulation Results Parameters		
Grid voltage amplitude	E_g	311 V
Reference load voltage amplitude	V_l^*	311 V
Grid and load fundamental frequency	f_o	60 Hz
Dc-link voltages	v_{Cj}	370 V
Grid filter inductors	L_g	3 mH
Load filter inductors	L_l	2 mH
Load filter capacitors	C_l	45 μF
Dc-link capacitors	C_{dc}	8.8 mF
PWM frequency	f_a	10 kHz
Load Power	P_l	10 kW
Experimental Results Parameters		
Grid voltage amplitude	E_g	155.56 V
Reference load voltage amplitude	V_l^*	155.56 V
Grid and load fundamental frequency	f_o	60 Hz
Dc-link voltages	v_{Cj}	160 V
Grid filter inductors	L_g	7 mH
Load filter inductors	L_l	2 mH
Load filter capacitors	C_l	45 μF
Dc-link capacitors	C_{dc}	4.5 mF
PWM frequency	f_a	10 kHz

7.5.2 Experimental Results

Fig. 7.12 shows the investigated converter operating during an unbalanced voltage sag. The disturbance consists of a single-phase sag in e_{g1} of 80%. From Figs. 7.12(a)-(c), the load perceives little disturbance, despite the voltage sag. Additionally, the dc-link voltages are properly regulated, as presented in Fig. 7.12(d). Fig. 7.13 shows experimental results for a load unbalanced transient from 1.0 kW to 2.0 kW. Firstly, Fig. 22(a) depicts the grid currents (i_{gj}) with zoomed view before the transient while Fig. 7.13(b) presents the grid currents (i_{gj}) with zoomed view after the transient. In Fig. 7.13(c) the load currents (i_{lj} and i_{l0}) with zoomed view in the period of the load change are presented. As can be seen in Fig. 7.13(d), dc-link voltages (v_{Cj}) kept controlled. Lastly, Fig. 7.14 presents

Figure 7.8 – Simulation result for a transient caused by a reduction of 33% in the nominal load power. (a) Grid voltages (e_{gj}). (b) Dc-link voltages (v_{Cj}). (c) Load currents (i_{lj}). (d) Grid currents (i_{gj}) before the transient. (e) Grid currents (i_{gj}). (f) Grid currents (i_{gj}) after the transient. (g) Load voltages (e_{lj}) before the transient. (h) Load voltages (e_{lj}). (i) Load voltages (e_{lj}) after the transient.

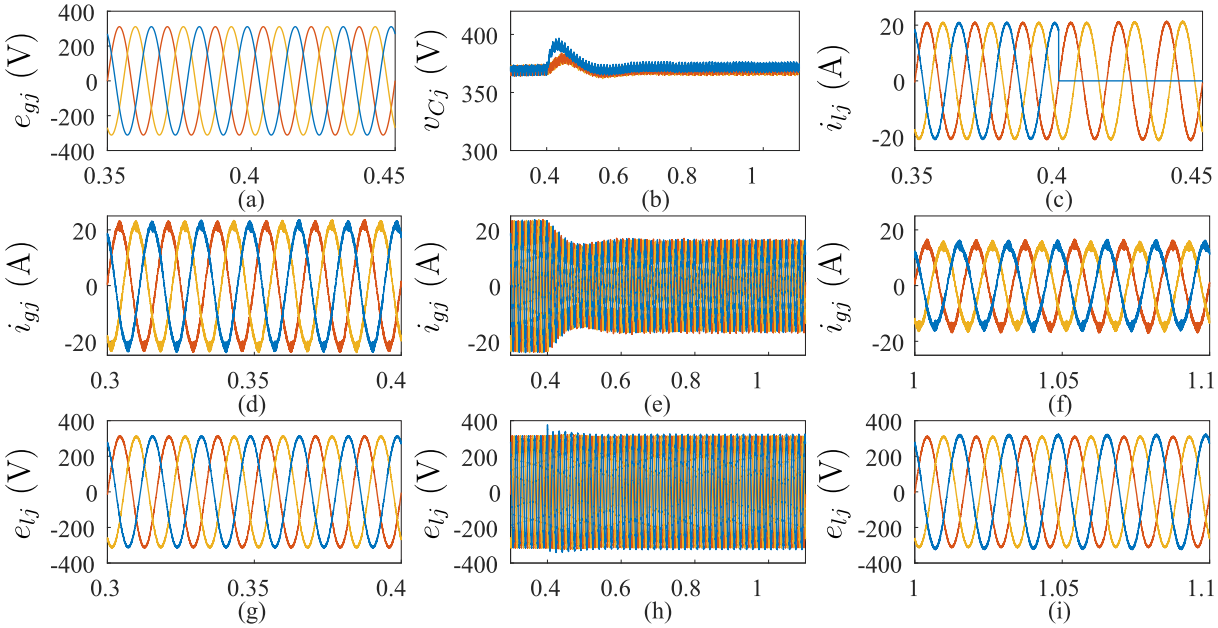
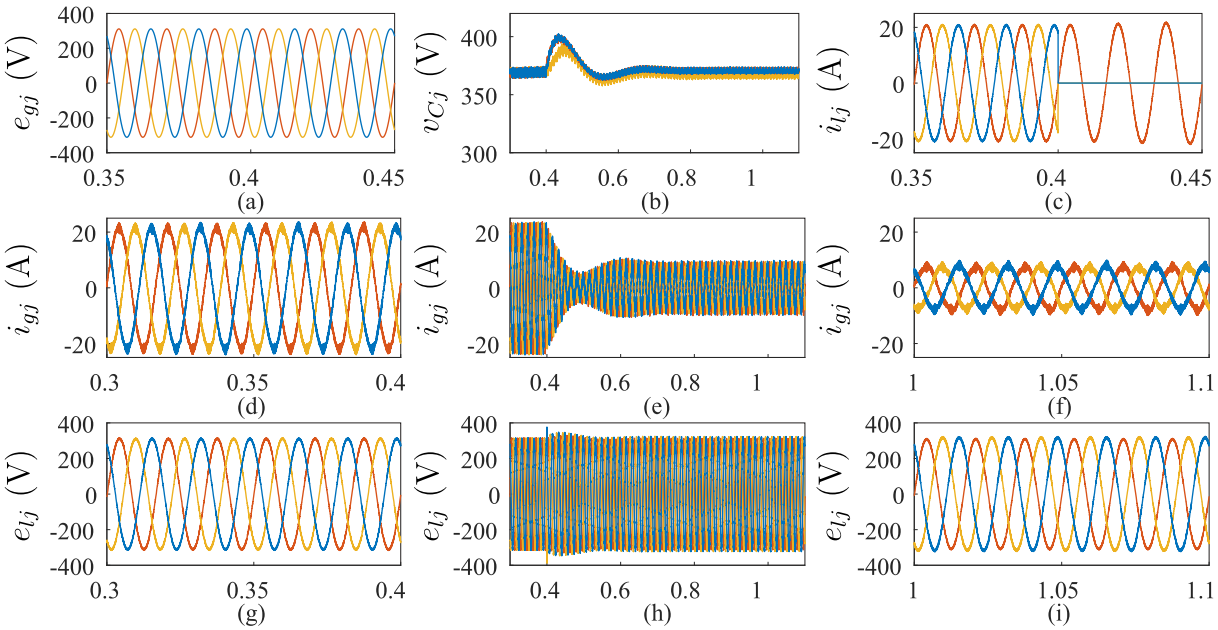


Figure 7.9 – Simulation result for a transient caused by a reduction of 66% in the nominal load power. (a) Grid voltages (e_{gj}). (b) Dc-link voltages (v_{Cj}). (c) Load currents (i_{lj}). (d) Grid currents (i_{gj}) before the transient. (e) Grid currents (i_{gj}). (f) Grid currents (i_{gj}) after the transient. (g) Load voltages (e_{lj}) before the transient. (h) Load voltages (e_{lj}). (i) Load voltages (e_{lj}) after the transient.



an experimental result with an unbalanced nonlinear load. The THD was measured for both load and grid currents. It can be seen that even though the load presents a harmonic distortion of 35%, the grid currents offer a sinusoidal and balanced waveform with a THD of 4.5%.

Figure 7.10 – Simulation result for a transient caused by single-phase fault in the grid voltage. (a) Grid voltages (e_{gj}). (b) Dc-link voltages (v_{Cj}). (c) Load currents (i_{lj}). (d) Grid currents (i_{gj}) before the transient. (e) Grid currents (i_{gj}). (f) Grid currents (i_{gj}) after the transient. (g) Load voltages (e_{lj}) before the transient. (h) Load voltages (e_{lj}). (i) Load voltages (e_{lj}) after the transient.

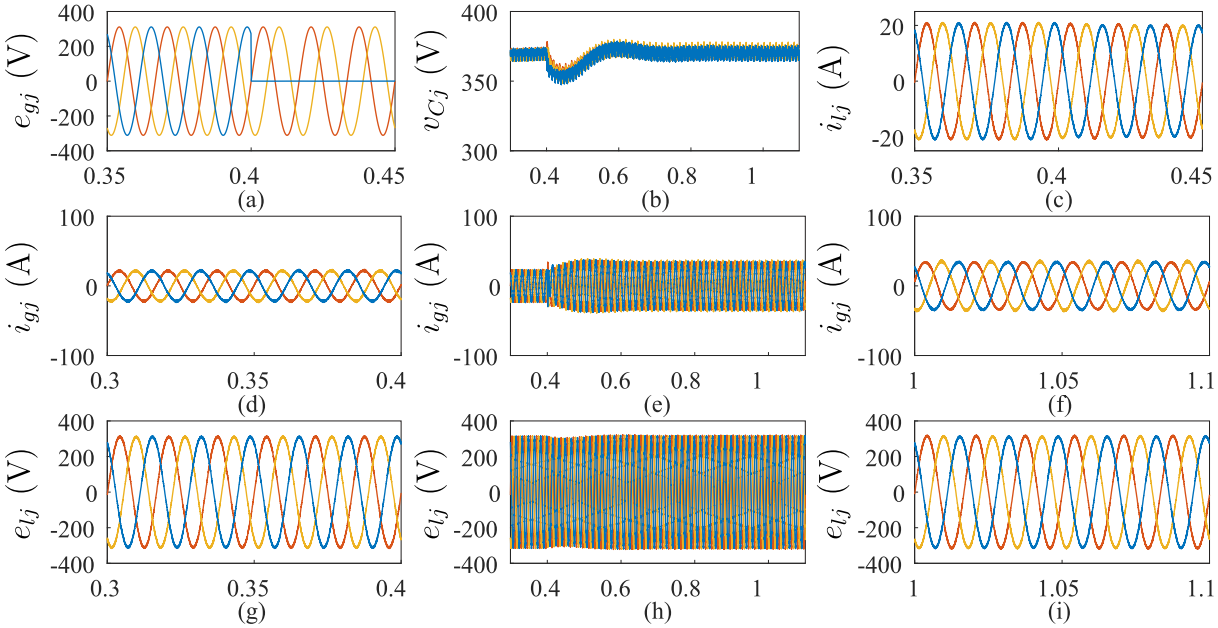


Figure 7.11 – Simulation result for a transient caused by two-phase fault in the grid voltage. (a) Grid voltages (e_{gj}). (b) Dc-link voltages (v_{Cj}). (c) Load currents (i_{lj}). (d) Grid currents (i_{gj}) before the transient. (e) Grid currents (i_{gj}). (f) Grid currents (i_{gj}) after the transient. (g) Load voltages (e_{lj}) before the transient. (h) Load voltages (e_{lj}). (i) Load voltages (e_{lj}) after the transient.

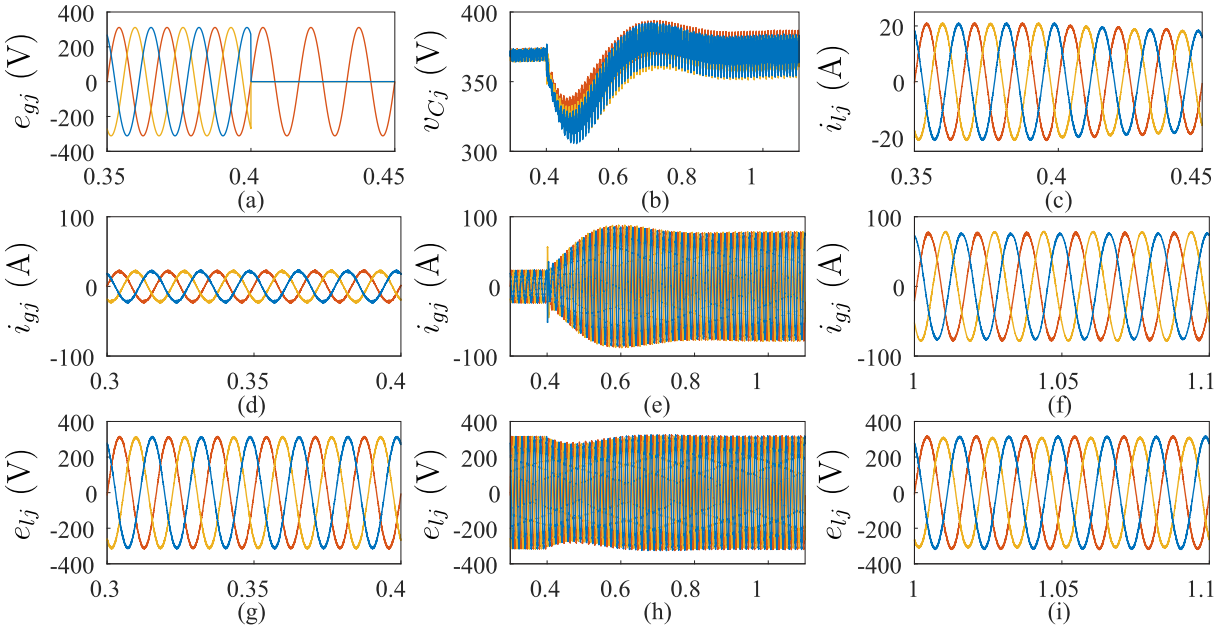


Figure 7.12 – Experimental results for an unbalanced grid voltage sag of 80% during 1 s. (a) Zoomed view before the transient of grid and load voltages. (b) Grid (e_{g1} and e_{g2}) and load (e_{l1} and e_{l2}) voltages. (c) Zoomed view after the transient of grid and load voltages. (d) DC-link voltages (v_{Cj}) and grid voltage e_{g1}

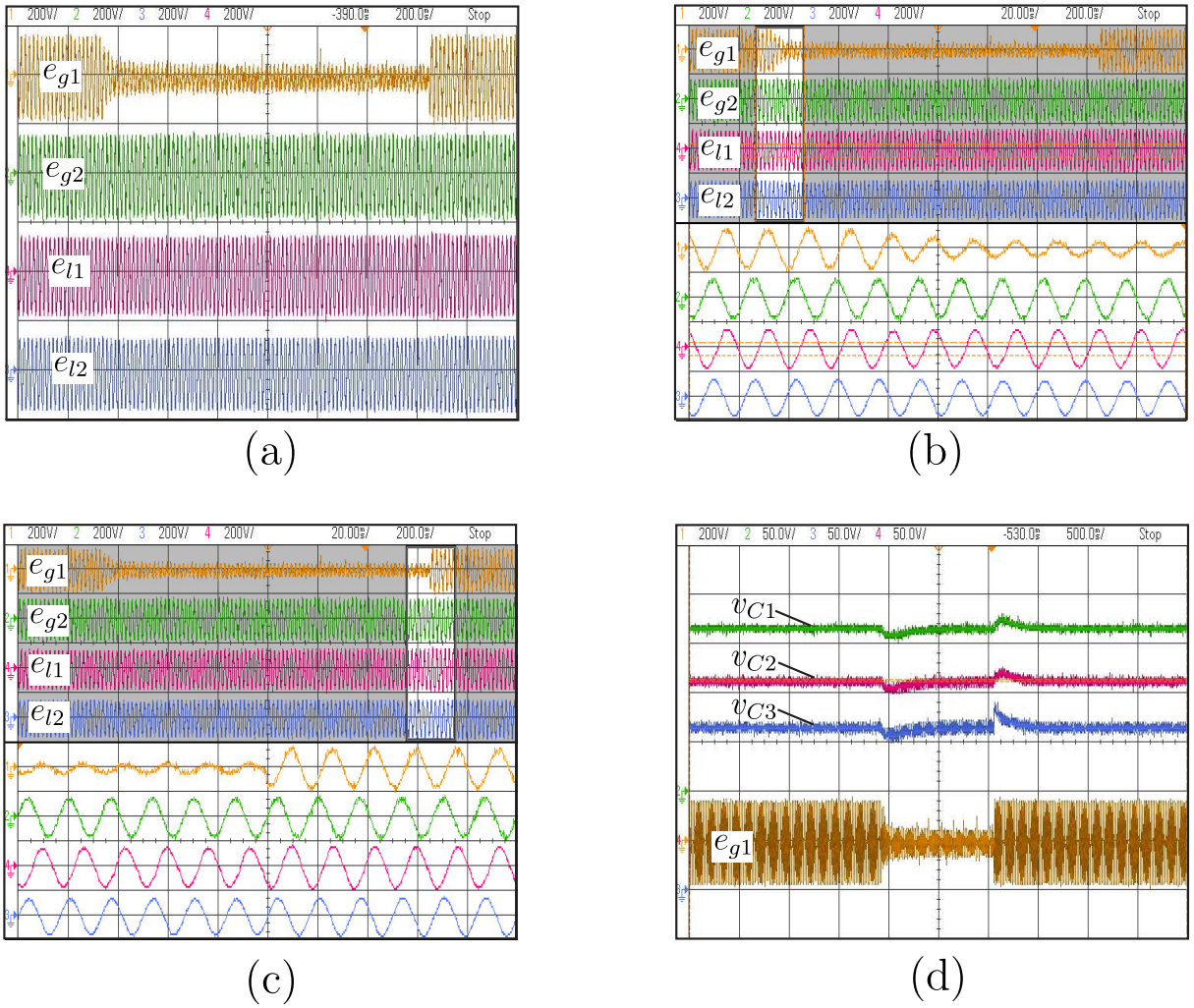
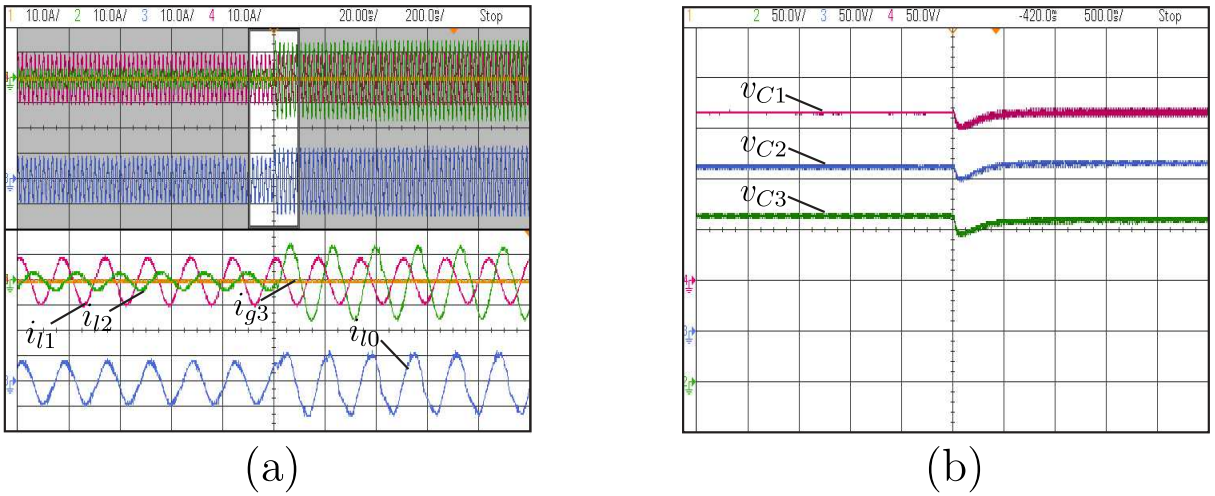


Figure 7.13 – Experimental results for a load unbalanced transient from 1.0 kW to 2.0 kW. (a) Grid currents (i_{gj}) with zoomed view before the transient. (b) Grid currents (i_{gj}) with zoomed view after the transient. (c) Load currents (i_{lj} and i_{l0}) with zoomed view in the period of the load change. (d) DC-link voltages (v_{Cj}).



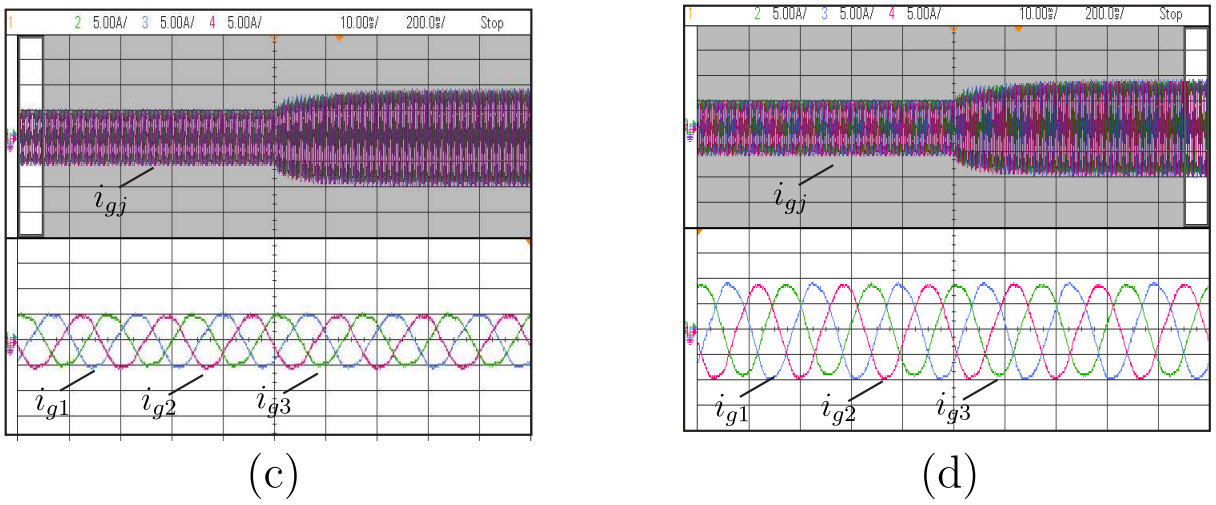
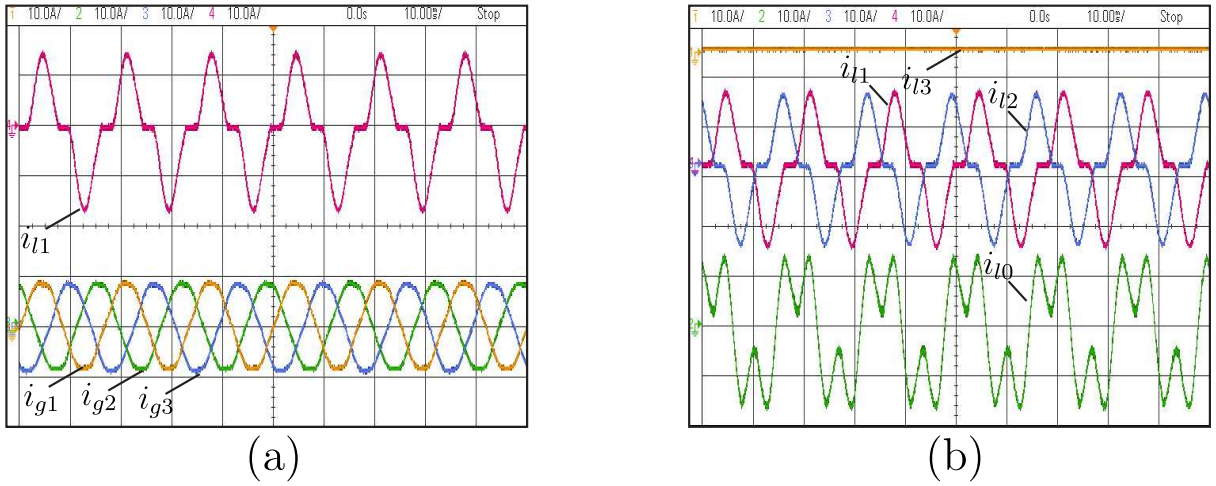


Figure 7.14 – Experimental results with an unbalanced nonlinear load.



7.6 Comparative Analysis

In this section, a further comparison between the investigated configuration and conventional solutions (KHADKIKAR, 2012; VENKATRAMAN; SELVAN, 2017; CHANG; CHANG; CHIANG, 2006; MAIA et al., 2018; TONGZHEN; JIN, 2014; KOROGLU et al., 2020; HAN et al., 2021) taking account the features summarized in the Table 7.3 are presented. Then, a comparative analysis of total harmonic distortion (THD) and semiconductor power losses is presented. The parameters used in tests for both studied topologies are addressed in Table 7.2, and in all analyses, it was considered an unbalanced load of 30%.

Compared with the most conventional UPQCs (KHADKIKAR, 2012), the investigated structure does not employ line-frequency transformers (LFT). The HFT-based solution presented in (KOROGLU et al., 2020) also employs LFTs. Not using LFTs contributes for increasing the power density and reducing the cost of the investigated configuration. Compared with the conventional transformerless solutions (VENKATRAMAN;

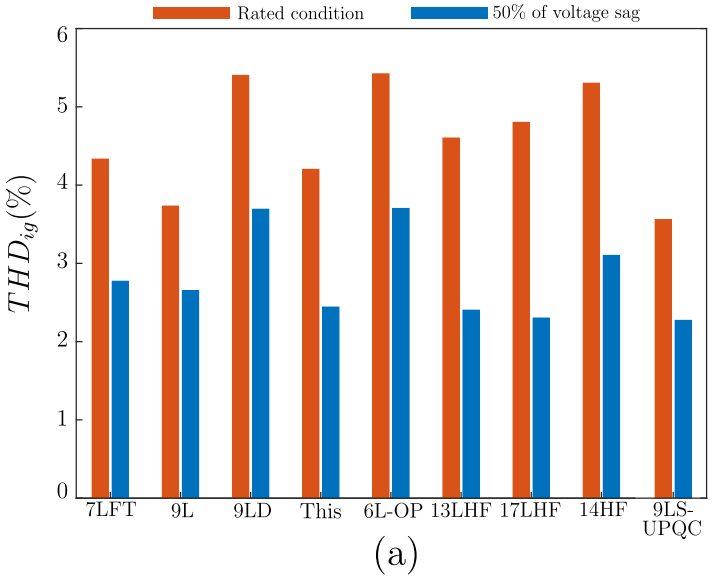
SELVAN, 2017; CHANG; CHANG; CHIANG, 2006; MAIA et al., 2018), the investigated configuration shows operational advantages. The investigated converter is able to compensate voltage sags maintaining a high grid power factor, different from (VENKATRAMAN; SELVAN, 2017). In addition, it can cope with any unbalanced conditions at both grid voltages and load voltages, which brings limitations for the dc-link balance control to the three-phase topology in (CHANG; CHANG; CHIANG, 2006). The investigated solution does not require open-ended connections at grid or load. This requirement imposes limitations regarding the application of the converter in (MAIA et al., 2018). Compared with the solutions based on high-frequency transformers (HFT) (TONGZHEN; JIN, 2014; HAN et al., 2021), the investigated converter requires fewer insulated gate bipolar transistors (IGBTs) and dc-link capacitors. In addition, if compared with the shunt dc-link voltage of (TONGZHEN; JIN, 2014; HAN et al., 2021), the investigated converter requires a reduced dc-link voltage and consequently switches with reduced reverse blocking voltage. To compare the totality of the required devices, the standing voltage of the converters was also evaluated, which is calculated as the sum of the reverse blocking voltage the converter IGBTs. For the values of Table 7.3, it was considered that the converters were able to compensate voltage sags of 50%. In this scenario, the investigated topology presented a lower standing voltage than the conventional HFT-based solutions (TONGZHEN; JIN, 2014; HAN et al., 2021). In this way, the investigated converter can represents a reduction in the cost of the converters compared with these converters.

The total harmonic distortion of the converters was evaluated considering the parameters presented in Table 7.2 and the minimum dc-link voltages described in Table 7.3. The THD can be calculated by

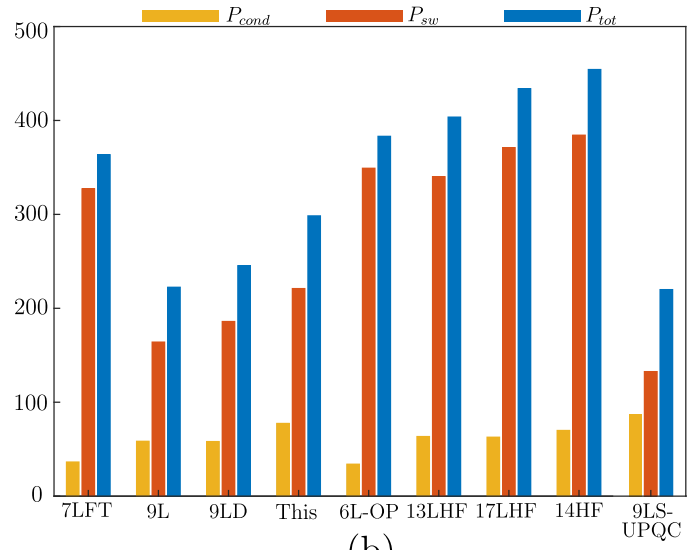
$$THD(\%) = \frac{100}{v_1}\sqrt{\sum_{u=2}^{N_u} v_u^2} \tag{7.23}$$

where v_1 is the amplitude of the fundamental component, v_u are the amplitudes of the harmonic components, u is the harmonic order and N_u is the number of considered harmonic components ($N_u = 1000$). Fig. 7.15(a) depicts the THD values for rated conditions and 50% of grid voltage sag. Notice that in both operation scenarios, the investigated converter presents lower harmonic content or similar values compared to the conventional solutions considered in the comparative analyses.

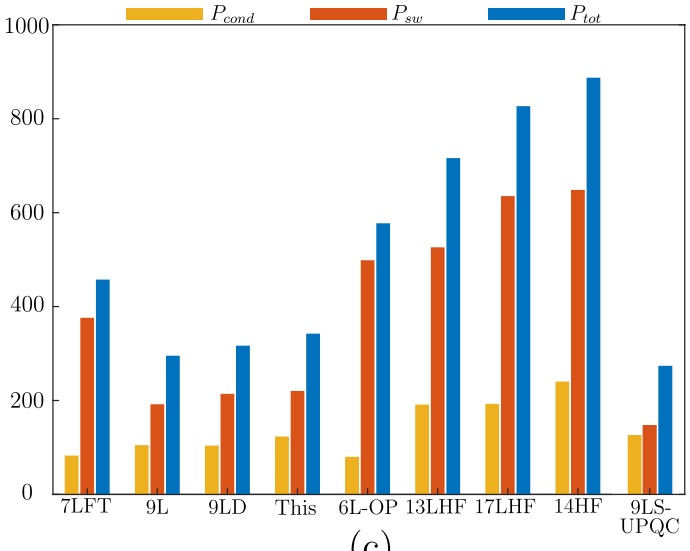
Figure 7.15 – Comparative analysis in terms of Total Harmonic Distortion and Power losses. (a) Total Harmonic distortion for rated conditions and 50% of grid voltage sag. (b) Power losses for rated conditions. (c) Power losses for 50% of grid voltage sag.



(a)



(b)



(c)

The power losses were evaluated using the thermal modules from PSIM software. The switching power modules selected for analysis was IGBT SKM50GB123D. The switching (P_{sw}), conduction (P_{cond}), and total power losses were done by choosing the THD value of the grid current equal to 5%, in which was acquired by setting the switching frequency of the shunt/series converter. The switching frequency of the high-frequency link (HFL) was kept at 10 kHz for all power losses analysis. As depicted in Fig. 7.15 (b-c), although the investigated topology presents higher conduction losses than those converters that do not use the HFL (KHADKIKAR, 2012; VENKATRAMAN; SELVAN, 2017; CHANG; CHANG; CHIANG, 2006; MAIA et al., 2018), it achieved lower switching losses compared to those that operate with HFL. In addition, taking into account the total power losses of the investigated converter, one can notice that the decrease in the switching losses compensates for the increase in the conduction losses. In this context, the investigated converter showed higher efficiency compared to (KHADKIKAR, 2012; VENKATRAMAN; SELVAN, 2017; TONGZHEN; JIN, 2014; KOROGLU et al., 2020; HAN et al., 2021). Compared to the transformerless 9LS-UPQC proposed in Chapter 6, the investigated configuration demonstrated higher losses. However, the 9LS-UPQC includes four additional inductors in its design, leading to a bulkier structure. Since power switches are generally less bulky than inductors, the HFT-based configuration investigated is more promising than 9LS-UPQC for applications where size and weight are critical considerations.

7.7 Conclusion

This work investigated an UQPC based on a nine-leg converter with shared legs connecting the three dc links by means of a dc-dc converter with a high-frequency transformer. Converter model, PWM technique, control strategy, steady-state analysis and experimental results were presented. The investigated converter does not present any line-frequency transformer, which allows size and cost reduction if compared with conventional UPQCs. It also presents advantages if compared with transformerless solutions, such as the capability of compensating voltage sags maintaining a high grid power factor without requiring additional dc sources, being able to operate under severe unbalanced conditions of grid voltage and load voltage and not requiring open-ended connection at grid or load. Compared with solutions based on high-frequency transformers it requires fewer dc-link capacitors and power switches and employing devices of reduced voltage rating.

Table 7.3 – Comparison of overall features with some available UPQCs. (E_g = 1 p.u. = 155.56 V)

Article	7LFT	6L-OP	9L	9LD	24HF	13LHF	17HF	This	9LS-UPQC
No LFT	✗	✓	✓	✓	✓	✗	✓	✓	✓
Voltage sag mitigation∗	✓	✗	✓	✓	✓	✓	✓	✓	✓
Unbalanced voltage mitigation	✓	✗	✗	✓	✓	✓	✓	✓	✓
Severely unbalanced load	✓	✓	✗	✓	✓	✓	✓	✓	✓
Grid and load in Y or Δ	✓	✓	✓	✗	✓	✓	✓	✓	✓
Number of IGBTs	14	12	18	18	48	26	34	30	26
Number of LFTs	3	0	0	0	0	3	0	0	0
Windings of the HFT	-	-	-	-	6	2	4	3	-
DC-link Capacitors	1	6	3	1	6	3	5	3	4
Shunt DC-link voltage (p.u.)	1.73	2.0	1.3	1.0	1.0	2.0	2.0	1.0	2.0
Series DC-link voltage (p.u.)	1.73	2.0	1.3	1.0	0.61	0.61	0.61	1.0	1.0
Standing Voltage (p.u.)	24.22	24.0	23.4	18.0	38.6	25.7	34.6	30.0	34.0

*In phase compensation

Chapter 8

Conclusion and Future Work

8.1 Conclusion

This research has studied eight ac-dc-ac configurations for UPQC applications. The contributions were made through the configurations that can demonstrate benefits in terms of semiconductor power losses, harmonic distortion, as well as improved series and shunt compensation compared to their conventional counterpart in some application scenarios.

In Chapter 2, a single-phase ac-dc-ac five-leg converter based on a high-frequency link was proposed. A further investigation into the operating ranges of the 5L-HFL is presented, which eliminates the need for voltage and current sensors to control the floating capacitor. Also, a comparison between the proposed 5L-LHF configuration and the 4L-HFL UQPC was addressed. In summary, the 5L-HFL converter has improvements over the 4L-HFL converter in terms of voltage ratings of the power devices, harmonic distortion, semiconductor power losses, and ac-filter size in high voltage low current applications. The comparative analysis indicated that the proposed 5L-HFL converter has lower total power losses than 4L-HFL, which were reduced by 5.7%, 16.6%, and 22.3% in scenarios with $\eta =$ 1, 2, and 3, respectively. Regarding ac-filter size, the 5L-HFL can reduce the inductance in up to 75% compared to the 4L-HFL. In addition, the proposed control system provided load voltage with fixed amplitude and frequency, unity grid power factor, and dc-link voltage regulation in scenarios with voltage sags, harmonic voltage, and reactive and harmonic currents. Since the HFL is unidirectional, the operation under grid voltage swells is not allowed. It was also found that the space vector plane becomes narrower, especially when $eta = 3$. In this context, the operation with $\eta = 2$ was chosen as the best of the three scenarios analyzed. When $\eta = 2$, the converter generates up to seven levels on the grid and load side. Also, in this scenario, there is a reasonable angle between the shunt

and series converter voltages, which allows the configuration to work properly.

In Chapter 3, a comprehensive investigation of a configuration that operates with a multilevel feature and achieves a reasonable voltage range to compensate for grid voltage harmonics, sags, and swells is presented. The proposed converter, named as 4L-PUC, allows one to compensate for grid voltage disturbances and nonactive load currents, being suitable in UPQC applications. A comparison between the proposed 4L-PUC configuration and the 4L converter was provided concerning the power processed by the transformer, rating of the semiconductor devices, harmonic distortion, power losses, and ac filter size. It can be highlighted that the proposed converter presented lower harmonic distortion with an improvement in the grid and load current THD up to 24% and 47%, respectively, compared to 4L. Additionally, the proposed one demonstrated a reduction of 50% in the output filter inductance compared to 4L converter. Regarding power losses, at least one leg of the 4L-PUC can operate at low frequency, reducing switching losses. The experimental efficiency of the 4L-PUC and 4L configurations were measured. It was verified that the proposed structure has better performance in high voltage and low current applications. The use of a LFT is the main drawback of the proposed 4L-PUC, especially when compared to HFT-based and transformerless solutions presented in the technical literature. On the other hand, as discussed in Chapter 3, the apparent power at the transformer of the proposed configuration is 42% lower than the conventional one.

In Chapter 4, new decoupling methods to improve the performance of single-phase transformerless UPQC based on three-leg and five-leg converters were investigated. In this context, three configurations were analyzed. First, a reconfiguration of the three-leg module using a bidirectional switch (3LS-UPQC) was proposed to improve voltage swell capability. Then, two five-leg configurations are studied, one based on three-leg and shunt modules (3LS-SH-UPQC) and another based on three-leg and standby converters (SB-3LS-UPQC). It was found that although 3LS-UPQC and SB-3LS-UPQC improved the operation over the conventional three-leg configuration, even so, issues related to the dependence on the load characteristics in the design of the dc-link voltage, which may result in an operation with low modulation index, was addressed. In this context, the proposed 3LS-SH-UPQC does not presented problems related to the dependence on the load characteristics since the hybrid shunt converter was responsible for compensating the harmonic and reactive power from the load. The power loss analysis showed that, although the proposed 3L-SH-UPQC has more semiconductor devices, it has better results than the conventional three-leg configuration and similar performance compared to 3LS-UPQC and SB-3LS-UPQC because the hybrid shunt enables low power consumption operation.

In Chapters 5, a single-phase transformerless UPQC based on two h-bridge modules (4L-UPQC) was proposed. In the proposed configuration, the way the load is connected allows the natural dc-link voltage balancing, which simplifies the design of the control

strategy compared to the conventional transformerless. A comparative analyzes in terms of semiconductor power losses between the proposed 4L-UPQC and 3LS-UPQC, SB-3LS-UPQC, and 3LS-SH-UPQC were made and it was found that, the proposed 4L-UPQC demonstrated a better performance under rated conditions and especially under grid voltage swell scenarios, presenting similar overall power losses than 3LS-UPQC and 3LS-SH-UPQC. On the other hand, this structure showed the worst results under all scenarios of grid voltage sags. This occurred because both structures, compared to 3LS-UPQC and 3LS-SH-UPQC, has more legs operating with the grid current. In this context, it was concluded that the proposed 4L-UQPC has a tendency to stand out in power losses under high voltage and low current scenarios. In addition, it was verified that although the decoupled method improves the overall performance of the three-leg converter, this approach increased the complexity of the control system. Therefore, the proposed 4L-UPQC is the most promising configuration presented in this work, as it does not have additional control loops or any other topological reconfiguration under transients.

Table 8.1 provides an overview of the characteristics of the UPQC systems studied in this work, evaluating them across key aspects such as operational features and component count. Although the 5L-HFL converter is the configuration with more semiconductor devices, the HFL allows asymmetrical dc-link and, consequently, operation with multilevel features in the grid and load sides. On the other hand, the phase angle limits between the shunt and series converter voltages must be respected to ensure proper operation. It has been noticed that the space-vector plane becomes narrower when the transformer turn ratio increases, reducing the voltage sag compensation capability. In addition, operation under grid voltage swells is not allowed for this configuration. Compared to the most conventional UPQC systems that employ line-frequency transformers, the proposed 4L-PUC demonstrated much better results regarding semiconductor power losses, harmonic distortion, and ac-filter size. However, line-frequency transformers are expensive components that often present high volume and weight, becoming a disadvantage compared to the transformerless configurations investigated in this work. Considering the transformerless configurations, as already mentioned, it was verified that although the decoupled method improves the overall performance of the three-leg converter over the conventional counterpart, this approach increases the complexity of the control system. In this way, the proposed 4L-UPQC is the most promising configuration studied here regarding the number of power switches and the overall control system.

In Chapter 6, a three-phase transformerless UPQC based on a nine-leg converter and a four-wire shunt converter (9LS) was proposed. The shunt converter converter provides balanced currents, which allows the nine-leg converter to operate with a wide range of unbalanced loads, while compensating harmonic content. In the comparative analysis it was found that the proposed 9LS has higher conduction losses than the conventional transformerless solutions (9L and 6L). However, it achieved better results in terms of

Table 8.1 – Comparison of overall features with some available transformerless UPQCs.

Configuration	5L-HFL	4L-PUC	3LS	SB-3LS	3LS-SH	4L-UPQC
Harmonic and reactive mit.	✓	✓	✓	✓	✓	✓
Voltage sag mitigation	✓	✓	✓	✓	✓	✓
Voltage swell mitigation	✗	✓	✓	✓	✓	✓
Number of IGBTs	14	10	7	10	11	8
Number of Diodes	4	0	4	0	4	0
Number of LFTs	0	1	0	0	0	0
Number of HFTs	1	0	0	0	0	0
Inductors and capacitors	3	3	3	3	5	3
Dc-link capacitors	2	2	1	2	1	2

switches losses. This occurred because the 9L and 6L structures operate with a dc-link voltage value higher than the proposed configuration. In addition, the shunt converter in the proposed converter was set to operate with a switching frequency five times lower than 9L and 6L. Therefore, the decrease in switching losses on the 9LS-UPQC compensated for the increase in the conduction losses. This indicates that the proposed converter is competitive in scenarios where switching losses are dominant.

Lastly, in Chapter 7, a three-phase four-wire converter consisting of a nine-leg converter and a bidirectional three-port dc-dc converter was investigated. This connection allowed the converter to operate with unbalanced power conditions as the TAB can redistribute power between the converter phases. A comparative analysis was performed considering some UPQC solutions available in the literature, such as LFT-based, HFT-based, and transformerless solutions. The investigated converter does not require line-frequency transformers, which enables a reduction in size and cost compared to conventional UPQCs. It also provides some advantages over transformerless solutions, such as the capability to compensate for voltage sags while maintaining a high grid power factor, without the need for additional dc sources. It can operate effectively under severe grid and load voltage unbalances and does not require an open-ended connection at the grid or load. Compared to solutions based on high-frequency transformers, it requires fewer dc-link capacitors and power switches, and it uses devices with a lower voltage rating. Compared to the transformerless 9LS-UPQC proposed in Chapter 6, the investigated configuration showed the worst loss results. On the other hand, 9LS-UPQC has four more inductors in its structure, which results in an increase in the structure's size and volume. Power switches are generally less bulky than inductors, in this way, the HFT-based configuration investigated is most promising for size- and weight-critical applications.

8.2 Future Work

Based on the studies presented in this work, the following topics can be developed in future work:

- Generalize the study of the 5L-HFL configuration considering 2 and 3 h-bridge modules connected to the common leg, with the aim to reduce the rating in the semiconductor devices;
- Generalize the study of the 4L-PUC configuration adding U cells in the grid and load side;
- Develop decoupling methods for three-phase UPQC systems, in order to increase the topology performance in terms of grid voltage swells;
- Apply the hybrid filter concept in the 3LS-UPQC converter to obtain better performances in terms of dc-link voltage;
- Propose control strategies for the 3LS-UPQC, 3LS-SH-UPQC, and SB-3LS-UPQC configurations in order to obtain better performances during the onset of the swell transient;
- Based on the 4L-UPQC configuration, propose multilevel topologies that can be used as statcom.

Appendix A

Inductor Filter Design

The minimum filter inductance was designed taking into account the maximum ripple of the current. Firstly, the analytical explanation was provided for a three-level voltage. Fig. A.1(a) illustrates the generated converter voltage and the filter inductance voltage (v_{L_l}).

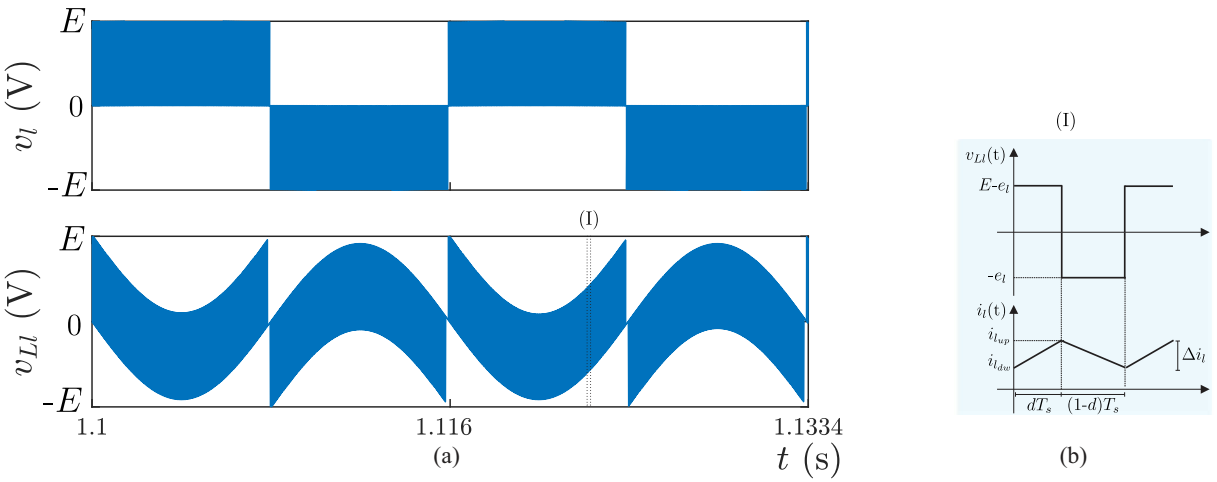


Figure A.1 – Idealized converter waveforms for the three-level voltage. (a) Generated converter voltage (v_l) and filter inductance voltage (v_{Ll}). (b) Zoom view of a switching period of the filter inductance voltage (v_{Ll}) and current (i_l).

From $v_{Ll} = v_l - e_l$ and analyzing only a positive half cycle of v_l, the filter inductance voltage is limited to $E - e_l$ and $-e_l$. Also, taking into account the switching period waveform shown in Fig. A.1(b), one can calculate the current ripple ($\Delta i_l = i_{l_{up}} - i_{l_{dw}}$). Since v_{Ll} presents a null average value in each switching period, the following equation can be derived

$$\int_0^{dT_s} (E - e_l)\, dt + \int_{dT_s}^{T_s} -e_l\, dt = 0, \tag{A.1}$$

where d is the duty cycle and T_s is the switching period. Assuming that $e_l = E_l \sin(\theta_l)$ with and the modulation index $m_l = E_l/E$, the following equation can be written from (A.1)

$$d = m_l \sin(\theta_l). \tag{A.2}$$

Since $v_{Ll} = L_l \frac{\Delta i_l}{\Delta t}$, considering the instant dT_s in which $v_{Ll} = E - e_l$, one can determine that

$$\frac{L_l \Delta i_l}{E T_s} = m_l \sin(\theta_l) - m_l^2 \sin^2(\theta_l). \tag{A.3}$$

The term $\frac{L_l \Delta i_l}{E T_s}$ related to (A.3) can be defined as the normalized current ripple, called $\overline{\Delta i_l}(m_l, \theta_l)$. Thus, it can be defined that

$$\overline{\Delta i_l}(m_l, \theta_l) = m_l \sin(\theta_l) - m_l^2 \sin^2(\theta_l). \tag{A.4}$$

Therefore, the minimum inductance value can be calculated considering the maximum normalized current ripple, as follows

$$L_l = \frac{E}{f_s \Delta i_l} \max[\overline{\Delta i_l}(m_l, \theta_l)]. \tag{A.5}$$

In this way, considering (A.4), the maximum normalized current ripple value can be evaluated according to the phase angle of the generated voltage for different modulation index values, as presented in Fig. A.2.

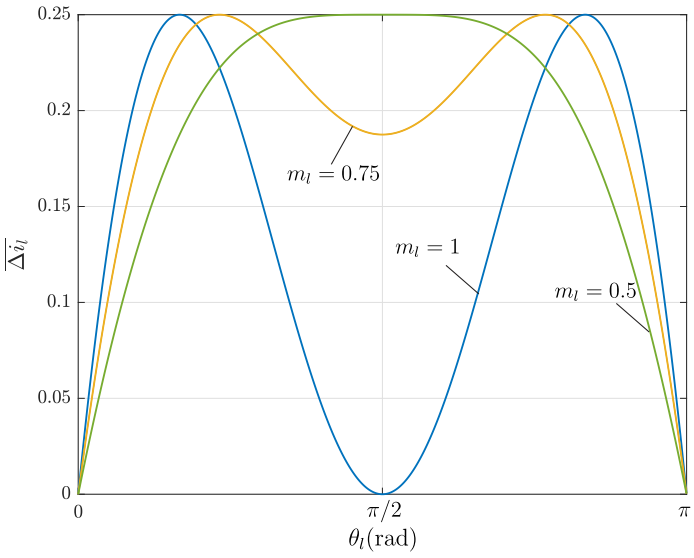


Figure A.2 – Profile of the normalized current ripple $\overline{\Delta i_l}$ according to the phase angle of the generated voltage and the modulation index - three-leg voltage.

Notice that, for any modulation index value higher than 0.5, the maximum normalized current ripple value is equal to 1/4. Therefore, the minimum inductance for three-level voltage can be computed as

$$L_l = \frac{E}{4\Delta i_l f_s}. \tag{A.6}$$

The minimum filter inductance for five-level voltage can be designed following the same methodology. Fig. A.3(a) shows that the structure synthesize five levels. Also, Figs. A.3 (b) and (c) show the filter inductance voltage waveform in a switching period considering the modulation index higher and lower than 0.5. Notice that the limits of v_{Ll} change for sector (I) and (II). In this context, the maximum current ripple should be evaluated in two steps considering the two sectors formed in a half cycle of v_l: (I): $m_l \geq 0.5$; (II): $m_l < 0.5$.

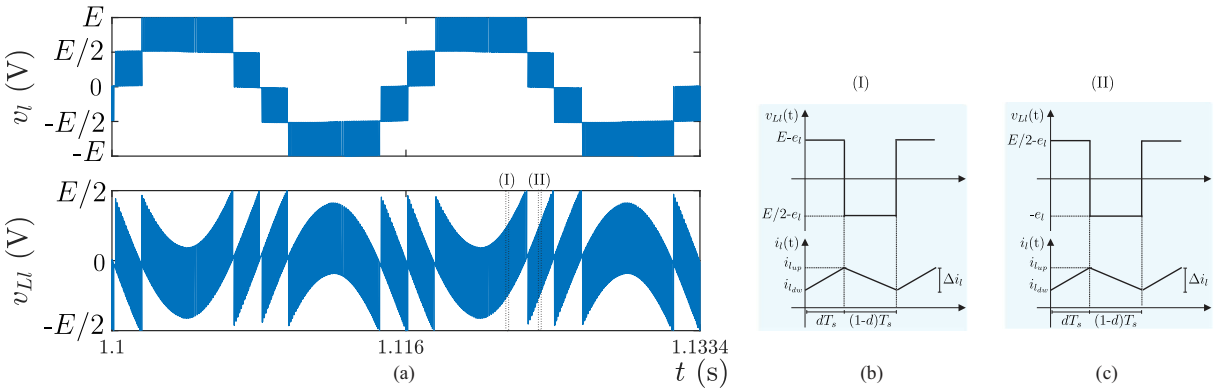


Figure A.3 – Idealized converter waveforms for the five-leg voltage. (a) Generated converter voltage (v_l) and filter inductance voltage (v_{Ll}). (b-c) Zoom view of a switching period of the filter inductance voltage (v_{Ll}) and current (i_l).

Firstly, for both sectors one can define

$$\frac{L_l \Delta i_l}{E T_s} = \begin{cases} 3m_l \sin(\theta_l) - 2m_l^2 \sin(\theta_l)^2 - 1, & m_l \geq 0.5 \\ \\ m_l \sin(\theta_l) - 2m_l^2 \sin^2(\theta_l), & m_l < 0.5 \end{cases} \tag{A.7}$$

and thus,

$$\overline{\Delta i_l}(m_l, \theta_l) = \begin{cases} 3m_l \sin(\theta_l) - 2m_l^2 \sin(\theta_l)^2 - 1, & m_l \geq 0.5 \\ m_l \sin(\theta_l) - 2m_l^2 \sin^2(\theta_l), & m_l < 0.5 \end{cases} \tag{A.8}$$

Therefore, the minimum inductance value can be also calculated as follows

$$L_l = \frac{E}{f_s \Delta i_l} \max[\overline{\Delta i_l}(m_l, \theta_l)]. \tag{A.9}$$

Fig. A.4 presents the profile of the normalized current ripple varying the generated voltage phase angle and the modulation index, considering (A.8). It can be noticed that for any modulation index higher than 0.5, the maximum normalized current ripple is equal to 1/8, thus, the minimum inductance value for five-level voltage can be computed as follows

$$L_l = \frac{E}{8\Delta i_l f_s}. \tag{A.10}$$

Comparing (A.6) and (A.10), it can be concluded that, for the same current ripple, the five-level voltage allows a reduction of 50% in size when compared with the three-level voltage.

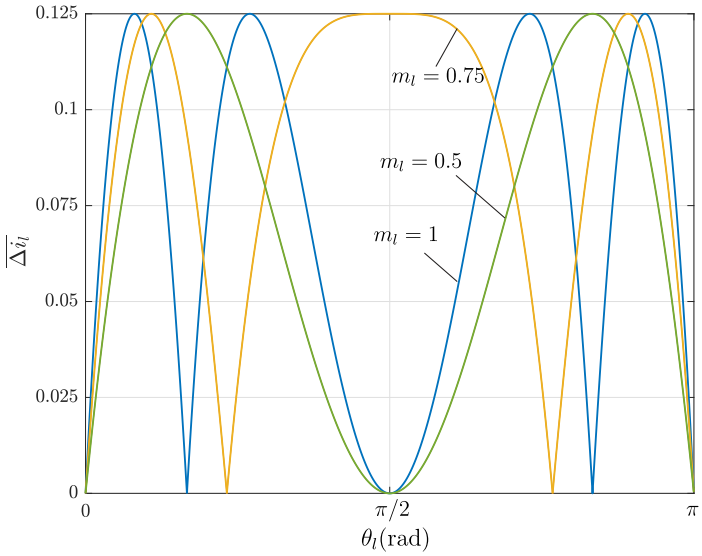


Figure A.4 – Profile of the normalized current ripple $\overline{\Delta i_l}$ according to the phase angle of the generated voltage and the modulation index - five-level voltage.

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